CC-218 Firmware Design

Contents:

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Summary

CC-218 FW is the firmware for CC-218.

Major features are:

- Control eVolume chip PGA2310
- Control display chip AS1115
- Read the position of the volume knob
- Control the relays of the selector
- Console function
- DVCS support
- IR remote support

Specifications

Hardware Specifications

MCU

MCU chip: PIC18F2520

Clock: 8MHz, internal clock oscillator

Reset: Internal

User manual: Microchip PICmicon_18Fxxxx.pdf

Port definition of MCU

Port	I/O	D/A	Name	Pin#	Function
A	I	A	AN0	2	Input from VR (analog)
	O	D	RA1	3	ZCEN (to PGA2310)
	O	D	RA2	4	nCS (to PGA2310)
	O	D	RA3	5	SCLK (to PGA2310)
	O	D	RA4	6	SDI (to PGA2310)
	I	D	RA5	7	SDO (from PGA2310)
	O	D	RA6	10	nMUTE (to PGA2310)
	O	D	RA7	9	(unused)
B	O	D	RB0	21	SEL_P
	O	D	RB1	22	SEL_D
	O	D	RB2	23	SEL_A
	O	D	RB3	24	(unused)
	I	D	RB4	25	nIR_IN (from TSOP34838)
	I	D	PGM	26	(unused, pulled down)
	I	D	PGC	27	Clock (from debugger)
	I/O	D	PGD	28	Data (to/from debugger)
C	O	D	RC0	11	(unused)
	O	D	RC1	12	nIRQ (from AS1115)
	O	D	CCP1	13	SQ_WAVE (10kHz square wave)
	O	D	SCL	14	Clock of I^2C (to AS1115)
	I/O	D	SDA	15	I^2C data/address (to/from AS1115)
	I	D	RC5	16	(unused)… used for test LED

	O	D	DVCS_TX	17	Async Tx of RS232C
	I	D	DVCS_RX	18	Async Rx of RS232C
E	I	P	VPP	1	Programing power (from debugger)

Interface with Peripherals

PGA2310

The signals ZCEN, nCS, SCLK, SDI, SDO, nMUTE are used to control PGA2310.
nCS, SCLK, SDI and SDO are used to communicate.
SDI (Serial Data Input) and SDO (Serial Data Output) are synchronized with SCLK.
nCS is chip select. It must be active low during communication.
ZCEN (Zero Cross Detection Enable) is used to minimize audible glitch when gain setting is changed.
Usually, ZCEN is kept active high.
nMute is used to mute.
Maybe, this signal is not used in this application. In that case, it is kept inactive high.

For further details, refer to the manual: TI PGA2310 (volume).pdf

AS1115

I^2C bus.

For further details, refer to the manual: AustriaMicrosystems_AS1115_DS000206_1-00(LedDriver).pdf

Console

RS232C asynchronous.
3-wire I/F: Tx, Rx, GND
19,200bps, 8-bit, 1 stop bit, no parity
EUSART of MCU chip is used.

IR Receiver

Receiver: Vishay TSOP34838
For details of the receiver, refer to the datasheet: Vishay_TSOP34838(IR_Receiver).pdf

Firmware Specifications

Soft real-time system.
Quasi-multitasking
Coded in C

Develop Environment

Integrated Development Environment: MPLAB X IDE v6.20

Compiler: XC8 v2.50

Debugging and programming: PICkit 5

Development Steps

Step-by-step approach is employed.

- Ver.0.0: Minimum feature… Make the LED on RC5 blink at 2Hz.
- Ver.0.1: UART driver added… Send “Hello world!” message to Console.
- Ver.0.2: Display feature added … Communicate w/ AS1115 via I^2C and display numbers on CC-218 DISP.
- Ver.0.3: VR interface added.
- Ver.0.4: Volume control feature added… Communicate w/ PGA3210 via serial port.
- Ver.0.5: Command feature added… CC-218 can be controlled by commands from Console.
- Ver.0.6: Infra-red interface added… Receive commands from IR remote.
- Ver.0.7: DVCS feature added… Control external device(s) via the serial port (DVCS).
- Ver.1.0: Release version

Ver.0.0

Ver.0.0 has a very simple feature: Blink LED connected to RC5 at 2Hz with 50% duty.
A simple feature has been added where RB2 (SEL_A) is driven together with the LED on RC5. [Ver.0.01]

These simple features are used to confirm basic functions of X IDE, PICkit 5 and target system (CC-218 MCU).

Configuration of MCU [v0.0]

Internal OSC used, WDT disabled and single-supply ICSP disabled.

Configuration Bits:

Name	Value	Field	Option	Category	Setting
ONFIG1H	8	-	-	-	-
	8	OSC	INTIO67	Oscillator Selection bits	Internal oscillator block port function on RA6 and RA7
	0	FCMEN	OFF	Fail-Safe Clock Monitor Enable bit	Fail-Safe Clock Monitor disabled
	0	IESO	OFF	Internal/External Oscillator Switchover bit	Oscillator Switchover mode disabled
CONFIG2L	1F	-	-	-	-
	1	PWRT	OFF	Power-up Timer Enable bit	PWRT disabled
	3	BOREN	SBORDIS	Brown-out Reset Enable bits	Brown-out Reset enabled in hardware only (SBOREN is disabled)
	3	BORV	3	Brown Out Reset Voltage bits	Minimum setting
CONFIG2H	1E	-	-	-	-
	0	WDT	OFF	Watchdog Timer Enable bit	WDT disabled (control is placed on the SWDTEN bit)
	F	WDTPS	32768	Watchdog Timer Postscale Select bits	1:32768
CONFIG3H	1	-	-	-	-
	1	CCP2MX	PORTC	CCP2 MUX bit	CCP2 input/output is multiplexed with RC1
	0	PBADEN	OFF	PORTB A/D Enable bit	PORTB<4:0> pins are configured as digital I/O on Reset
	0	LPT1OSC	OFF	Low-Power Timer1 Oscillator Enable bit	Timer1 configured for higher power operation
	0	MCLRE	OFF	MCLR Pin Enable bit	RE3 input pin enabled; MCLR disabled
CONFIG4L	81	-	-	-	-
	1	STVREN	ON	Stack Full/Underflow Reset Enable bit	Stack full/underflow will cause Reset
	0	LVP	OFF	Single-Supply ICSP Enable bit	Single-Supply ICSP disabled
	0	XINST	OFF	Extended Instruction Set Enable bit	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
CONFIG5L	0F	-	-	-	-
	1	CP0	OFF	Code Protection bit	Block 0 (000800-001FFFh) not code-protected
	1	CP1	OFF	Code Protection bit	Block 1 (002000-003FFFh) not code-protected
	1	CP2	OFF	Code Protection bit	Block 2 (004000-005FFFh) not code-protected
	1	CP3	OFF	Code Protection bit	Block 3 (006000-007FFFh) not code-protected
CONFIG5H	C0	-	-	-	-
	1	CPB	OFF	Boot Block Code Protection bit	Boot block (000000-0007FFh) not code-protected
	1	CPD	OFF	Data EEPROM Code Protection bit	Data EEPROM not code-protected
ONFIG6L	0F	-	-	-	-
	1	WRT0	OFF	Write Protection bit	Block 0 (000800-001FFFh) not write-protected
	1	WRT1	OFF	Write Protection bit	Block 1 (002000-003FFFh) not write-protected
	1	WRT2	OFF	Write Protection bit	Block 2 (004000-005FFFh) not write-protected
	1	WRT3	OFF	Write Protection bit	Block 3 (006000-007FFFh) not write-protected

CONFIG6H	E0	-	-	-	-
	1	WRTC	OFF	Configuration Register Write Protection bit	Configuration registers (300000-3000FFh) not write-protected
	1	WRTB	OFF	Boot Block Write Protection bit	Boot block (000000-0007FFh) not write-protected
	1	WRTD	OFF	Data EEPROM Write Protection bit	Data EEPROM not write-protected
CONFIG7L	0F	-	-	-	-
	1	EBTR0	OFF	Table Read Protection bit	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks
	1	EBTR1	OFF	Table Read Protection bit	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks
	1	EBTR2	OFF	Table Read Protection bit	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks
	1	EBTR3	OFF	Table Read Protection bit	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks
ONFIG7H	40	EBTRB	OFF	Boot Block Table Read Protection bit	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

SFR settings [v0.0]

Address	Name	R/W	Hex	Binary	Description
F80	PORTA	R	00	0000 0000	Status of Port A pins. Always 00h because Port A is disabled.
F81	PORTB	R	00	0000 0000	Status of Port B pins. Always 00h because Port B is disabled.
F82	PORTC	R	x0	00x0 0000	Status of Port C pins. Bit 5 is controlled by F/W. The other bits are always '0'
F84	PORTE	R	00	0000 0000	Status of Port E pins. Always 00h because Port E is disabled.
F89	LATA	R/W	00	0000 0000	Latch for Port A. Unused (default).
F8A	LATB	R/W	0X	0000 0x00	Latch for Port B. Alternate RB2 output.
F8B	LATC	R/W	x0	00x0 0000	Latch for Port C. RC5 is used to blink LED.
F92	TRISA	W	FF	1111 1111	All output buffers in tri-state (this port is input)(default).
F93	TRISB	W	FB	1111 1011	All output buffers but RB2 in tri-state (RB2 is output)
F94	TRISC	W	DF	1101 1111	All output buffers but RC5 in tri-state (RC5 is output).
F9B	OSCTUNE	W	00	0000 0000	Default
F9D	PIE1	W	00	0000 0000	All peripheral interrupts inhibited… Default
F9E	PIR1	R	00	0000 0000	Peripheral interrupt request flag
F9F	IPR1	W	FF	1111 1111	Peripheral interrupt priority… Default
FA0	PIE2	W	00	0000 0000	All peripheral interrupts inhibited… Default
FA1	PIR2	R	00	0000 0000	Peripheral interrupt request flag
FA2	IPR2	W	FF	1111 1111	Peripheral interrupt priority… Default
FA6	EECON1	-	xx	xxxx xxxx	EEPROM control… Don' t access
FA7	EECON2	-	xx	xxxx xxxx	EEPROM control… Don' t access
FA8	EEDATA	-	xx	xxxx xxxx	EEPROM data… Don' t access
FA9	EEADR	-	xx	xxxx xxxx	EEPROM address… Don' t access
FAB	RCSTA	W	00	0000 0000	Serial port receive status and control… Serial port disable
FAC	TXSTA	W	00	0000 0000	Serial port transmit status and control… Transmit disable
FAD	TXREG	-	xx	xxxx xxxx	EUSART transmit register… Don' t access
FAE	RCREG	-	xx	xxxx xxxx	EUSART receive register… Don' t access
FAF	SPBRG	-	xx	xxxx xxxx	Serial port baud rate generator… Don' t access
FB0	SPBRGH	-	xx	xxxx xxxx	Serial port baud rate generator high byte… Don' t access
FB1	T3CON	W	00	0000 0000	Timer control… default
FB2	TMR3L	-	xx	xxxx xxxx	Timer3 register low byte… Don' t access
FB3	TMR3H	-	xx	xxxx xxxx	Timer3 register high byte… Don' t access
FB4	CMCON	W	07	0000 0111	Comparator control… Default
FB5	CVRCON	W	00	0000 0000	Comparator voltage reference… Default
FB6	ECCP1AS	W	00	0000 0000	ECCP auto-shutdown control… Default
FB7	PWM1CON	W	00	0000 0000	PWM dead-band delay… Default
FB8	BAUDCON	W	00	0000 0000	Baud rate control… Default
FBA	CCP2CON	-	xx	xxxx xxxx	CCP2 control… Don' t access
FBB	CCPR2L	-	xx	xxxx xxxx	Capture/compare/PWM register 2 low byte… Don' t access
FBC	CCPR2H	-	xx	xxxx xxxx	Capture/compare/PWM register 2 high byte… Don' t access
FBD	CCP1CON	-	xx	xxxx xxxx	CCP1 control… Don' t access
FBE	CCPR1L	-	xx	xxxx xxxx	Capture/compare/PWM register 1 low byte… Don' t access
FBF	CCPR1H	-	xx	xxxx xxxx	Capture/compare/PWM register 1 high byte… Don' t access
FC0	ADCON2	W	00	0000 0000	A/D control 2
FC1	ADCON1	W	00	0000 0000	A/D control 1
FC2	ADCON0	W	00	0000 0000	A/D control 0
FC3	ADRESL	-	xx	xxxx xxxx	A/D result low byte… Don' t access
FC4	ADRESH	-	xx	xxxx xxxx	A/D result high byte… Don' t access
FC5	SSPCON2	W	00	0000 0000	MSSP control 2 (I^2C)… Default (disable)
FC6	SSPCON1	W	00	0000 0000	MSSP control 1 (SPI)… Default (disable)
FC7	SSPSTAT	R	xx	xxxx xxxx	MSSP status (I^2C)… Don' t access
FC8	SSPADD	-	xx	xxxx xxxx	MSSP address (I^2C slave)… Don' t access
FC9	SSPBUF	-	xx	xxxx xxxx	MSSP Receive/Transmit buffer… Don' t access
FCA	T2CON	W	00	0000 0000	Timer2 control… Default (disable)

FCB	PR2	–	xx	xxxx xxxx	Timer2 period… Don’ t access
FCC	TMR2	–	xx	xxxx xxxx	Timer2… Don’ t access
FCD	T1CON	W	00	0000 0000	Timer1 control… Default (disable)
FCE	TMR1L	–	xx	xxxx xxxx	Timer1 low byte… Don’ t access
FCF	TMR1H	–	xx	xxxx xxxx	Timer1 high byte… Don’ t access
FD0	RCON	–	xx	xxxx xxxx	Reset control… Don’ t access
FD1	WDTCON	W	00	0000 0000	Watch dog timer control… Default (disable)
FD2	HLVDCON	W	05	0000 0101	High/low voltage detect control… Default (disable)
FD3	OSCCON	R/W	72	0111 0010	Oscillator control… Internal oscillator, 8MHz
FD5	T0CON	W	4F	0100 1111	Timer0 control… Disable
FD6	TMR0L	–	xx	xxxx xxxx	Timer0 low byte… Don’ t access
FD7	TMR0H	–	xx	xxxx xxxx	Timer0 high byte… Don’ t access
FD8	STATUS	R	xx	xxxx xxxx	Status… Don’ t access
FD9	FSR2L	–	xx	xxxx xxxx	FSR2 (Data memory pointer) low byte… Don’ t access
FDA	FSR2H	–	xx	xxxx xxxx	FSR2 (Data memory pointer) high byte… Don’ t access
FDB	PLUSW2	–	xx	xxxx xxxx	Not physical register
FDC	PREINC2	–	xx	xxxx xxxx	Not physical register
FDD	POSTDEC2	–	xx	xxxx xxxx	Not physical register
FDE	POSTINC2	–	xx	xxxx xxxx	Not physical register
FDF	INDF2	–	xx	xxxx xxxx	Not physical register
FE0	BSR	–	xx	xxxx xxxx	Bank select… Don’ t access
FE1	FSR1L	–	xx	xxxx xxxx	FSR1 (Data memory pointer) low byte… Don’ t access
FE2	FSR1H	–	xx	xxxx xxxx	FSR1 (Data memory pointer) high byte… Don’ t access
FE3	PLUSW1	–	xx	xxxx xxxx	Not physical register
FE4	PREINC1	–	xx	xxxx xxxx	Not physical register
FE5	POSTDEC1	–	xx	xxxx xxxx	Not physical register
FE6	POSTINC1	–	xx	xxxx xxxx	Not physical register
FE7	INDF1	–	xx	xxxx xxxx	Not physical register
FE8	WREG	–	xx	xxxx xxxx	Working register… Don’ t access
FE9	FSR0L	–	xx	xxxx xxxx	FSR0 (Data memory pointer) low byte… Don’ t access
FEA	FSR0H	–	xx	xxxx xxxx	FSR0 (Data memory pointer) high byte… Don’ t access
FEB	PLUSW0	–	xx	xxxx xxxx	Not physical register
FEC	PREINC0	–	xx	xxxx xxxx	Not physical register
FED	POSTDEC0	–	xx	xxxx xxxx	Not physical register
FEE	POSTINC0	–	xx	xxxx xxxx	Not physical register
FEF	INDF0	–	xx	xxxx xxxx	Not physical register
FF0	INTCON3	W	C0	1100 0000	External interrupt control… disable(default)
FF1	INTCON2	W	F5	1111 0101	External and Timer0 interrupt control… Default
FF2	INTCON	W	00	0000 0000	Interrupt control… disable(default)
FF3	PRODL	–	xx	xxxx xxxx	Product of multiply low byte… Don’ t access
FF4	PRODH	–	xx	xxxx xxxx	Product of multiply low byte… Don’ t access
FF5	TABLAT	–	xx	xxxx xxxx	Program memory table latch… Don’ t access
FF6	TBLPTRL	–	xx	xxxx xxxx	Program memory table pointer low byte… Don’ t access
FF7	TBLPTRH	–	xx	xxxx xxxx	Program memory table pointer high byte… Don’ t access
FF8	TBLPTRU	–	xx	xxxx xxxx	Program memory table pointer upper byte… Don’ t access
FF9	PCL	–	xx	xxxx xxxx	Program counter low byte (also defined as PCLAT)… Don’ t access
FFA	PCLATH	–	xx	xxxx xxxx	Program counter latch low byte… Don’ t access
FFB	PCLATU	–	xx	xxxx xxxx	Program counter latch upper byte… Don’ t access
FFC	STKPTR	–	xx	xxxx xxxx	Stack pointer… Don’ t access
FFD	TOSL	–	xx	xxxx xxxx	Top-of-stack low byte… Don’ t access
FFE	TOSH	–	xx	xxxx xxxx	Top-of-stack high byte… Don’ t access
FFF	TOSU	–	xx	xxxx xxxx	Top-of-stack upper byte… Don’ t access

Source Files [v0.0]

Module	Source	Header	Description
MAIN	main.c V0.00 V0.01	main.h V0.00 V0.01	Main function Version history
INIT	init.c V0.00	init.h V0.00 V0.01	Initialize SEL_A output (relay drive signal)
DIAG	diag.c V0.00 V0.01	diag.h V0.00	Diagnostics… Blink LED Drive relays (BD4: RL5-6)

Ver.0.1

UART driver added.
Ver.0.10: Send opening message “CC-218 FW Ver.0.10” to Console.
Ver.0.11: Interrupt is used.
Ver.0.12: Receive characters from Console and echo them back.

Specifications

EUSART is used as UART (asynchronous mode).
Baud rate: 19,200 baud
This driver collaborates with putch() function in the standard library.
The standard functions printf() can be used by the application; i.e. formatted texts can be transmitted.
Interrupt is used for both transmit (TXREG empty) and receive (RXREG full).

Configuration of MCU [v0.1]

Internal OSC used, WDT disabled and single-supply ICSP disabled.
Same as Ver.0.0.

SFR settings [v0.1]

Address	Name	R/W	Hex	Binary	Description
F80	PORTA	R	00	0000 0000	Status of Port A pins. Always 00h because Port A is disabled.
F81	PORTB	R	00	0000 0000	Status of Port B pins. Always 00h because Port B is disabled.
F82	PORTC	R	x0	00x0 0000	Status of Port C pins. Bit 5 is controlled by F/W. The other bits are always ‘0’
F84	PORTE	R	00	0000 0000	Status of Port E pins. Always 00h because Port E is disabled.
F89	LATA	R/W	00	0000 0000	Latch for Port A. Unused (default).
F8A	LATB	R/W	0X	0000 0x00	Latch for Port B. Alternate RB2 output.
F8B	LATC	R/W	x0	00x0 0000	Latch for Port C. RC5 is used to blink LED.
F92	TRISA	W	FF	1111 1111	All output buffers in tri-state (this port is input)(default).
F93	TRISB	W	FB	1111 1011	All output buffers but RB2 in tri-state (RB2 is output)
F94	TRISC	W	DF	1101 1111	All output buffers but RC5 in tri-state (RC5 is output).
F9B	OSCTUNE	W	00	0000 0000	Default
F9D	PIE1	W	30	0011 0000	Rx/Tx int enable
F9E	PIR1	R	00	0000 0000	Peripheral interrupt request flag
F9F	IPR1	W	CF	1100 1111	Peripheral interrupt priority… UART in low priority
FA0	PIE2	W	00	0000 0000	All peripheral interrupts inhibited… Default
FA1	PIR2	R	00	0000 0000	Peripheral interrupt request flag
FA2	IPR2	W	FF	1111 1111	Peripheral interrupt priority… Default
FA6	EECON1	-	xx	xxxx xxxx	EEPROM control… Don’t access
FA7	EECON2	-	xx	xxxx xxxx	EEPROM control… Don’t access
FA8	EEDATA	-	xx	xxxx xxxx	EEPROM data… Don’t access
FA9	EEADR	-	xx	xxxx xxxx	EEPROM address… Don’t access
FAB	RCSTA	W	90	1001 0000	Serial port receive status and control… Serial port enable

FAC	TXSTA	W	26	0010 0110	Serial port transmit status and control… Transmit disable Bit-5 (TXEN) is set after related registers are initialized)
FAD	TXREG	W	xx	xxxx xxxx	EUSART transmit register
FAE	RCREG	R	xx	xxxx xxxx	EUSART receive register
FAF	SPBRG	W	19	0001 1001	Serial port baud rate generator… 25(=19h):19,200bps *1
FB0	SPBRGH	–	xx	xxxx xxxx	Serial port baud rate generator high byte… Don't access
FB1	T3CON	W	00	0000 0000	Timer control… default
FB2	TMR3L	–	xx	xxxx xxxx	Timer3 register low byte… Don't access
FB3	TMR3H	–	xx	xxxx xxxx	Timer3 register high byte… Don't access
FB4	CMCON	W	07	0000 0111	Comparator control… Default
FB5	CVRCON	W	00	0000 0000	Comparator voltage reference… Default
FB6	ECCP1AS	W	00	0000 0000	ECCP auto-shutdown control… Default
FB7	PWM1CON	W	00	0000 0000	PWM dead-band delay… Default
FB8	BAUDCON	W	02	0000 0010	Baud rate control… Enable receive wake-up
FBA	CCP2CON	–	xx	xxxx xxxx	CCP2 control… Don't access
FBB	CCPR2L	–	xx	xxxx xxxx	Capture/compare/PWM register 2 low byte… Don't access
FBC	CCPR2H	–	xx	xxxx xxxx	Capture/compare/PWM register 2 high byte… Don't access
FBD	CCP1CON	–	xx	xxxx xxxx	CCP1 control… Don't access
FBE	CCPR1L	–	xx	xxxx xxxx	Capture/compare/PWM register 1 low byte… Don't access
FBF	CCPR1H	–	xx	xxxx xxxx	Capture/compare/PWM register 1 high byte… Don't access
FC0	ADCON2	W	00	0000 0000	A/D control 2
FC1	ADCON1	W	00	0000 0000	A/D control 1
FC2	ADCON0	W	00	0000 0000	A/D control 0
FC3	ADRESL	–	xx	xxxx xxxx	A/D result low byte… Don't access
FC4	ADRESH	–	xx	xxxx xxxx	A/D result high byte… Don't access
FC5	SSPCON2	W	00	0000 0000	MSSP control 2 (I^2C)… Default (disable)
FC6	SSPCON1	W	00	0000 0000	MSSP control 1 (SPI)… Default (disable)
FC7	SSPSTAT	R	xx	xxxx xxxx	MSSP status (I^2C)… Don't access
FC8	SSPADD	–	xx	xxxx xxxx	MSSP address (I^2C slave)… Don't access
FC9	SSPBUF	–	xx	xxxx xxxx	MSSP Receive/Transmit buffer… Don't access
FCA	T2CON	W	00	0000 0000	Timer2 control… Default (disable)
FCB	PR2	–	xx	xxxx xxxx	Timer2 period… Don't access
FCC	TMR2	–	xx	xxxx xxxx	Timer2… Don't access
FCD	T1CON	W	00	0000 0000	Timer1 control… Default (disable)
FCE	TMR1L	–	xx	xxxx xxxx	Timer1 low byte… Don't access
FCF	TMR1H	–	xx	xxxx xxxx	Timer1 high byte… Don't access
FD0	RCON	W	DF	1101 1111	Reset control… Enable interrupt priority level
FD1	WDTCON	W	00	0000 0000	Watch dog timer control… Default (disable)
FD2	HLVDCON	W	05	0000 0101	High/low voltage detect control… Default (disable)
FD3	OSCCON	R/W	72	0111 0010	Oscillator control… Internal oscillator, 8MHz
FD5	T0CON	W	D3	1101 0011	Timer0 control… Enable, 8-bit, 1/16 prescale *2
FD6	TMR0L	W	81	1000 0011	Timer0 low byte… 1msec interval *1
FD7	TMR0H	–	xx	xxxx xxxx	Timer0 high byte… Don't access
FD8	STATUS	R	xx	xxxx xxxx	Status… Don't access
FD9	FSR2L	–	xx	xxxx xxxx	FSR2 (Data memory pointer) low byte… Don't access
FDA	FSR2H	–	xx	xxxx xxxx	FSR2 (Data memory pointer) high byte… Don't access
FDB	PLUSW2	–	xx	xxxx xxxx	Not physical register
FDC	PREINC2	–	xx	xxxx xxxx	Not physical register
FDD	POSTDEC2	–	xx	xxxx xxxx	Not physical register
FDE	POSTINC2	–	xx	xxxx xxxx	Not physical register
FDF	INDF2	–	xx	xxxx xxxx	Not physical register
FE0	BSR	–	xx	xxxx xxxx	Bank select… Don't access
FE1	FSR1L	–	xx	xxxx xxxx	FSR1 (Data memory pointer) low byte… Don't access
FE2	FSR1H	–	xx	xxxx xxxx	FSR1 (Data memory pointer) high byte… Don't access
FE3	PLUSW1	–	xx	xxxx xxxx	Not physical register
FE4	PREINC1	–	xx	xxxx xxxx	Not physical register
FE5	POSTDEC1	–	xx	xxxx xxxx	Not physical register

FE6	POSTINC1	-	xx	xxxx xxxx	Not physical register
FE7	INDF1	-	xx	xxxx xxxx	Not physical register
FE8	WREG	-	xx	xxxx xxxx	Working register… Don't access
FE9	FSR0L	-	xx	xxxx xxxx	FSR0 (Data memory pointer) low byte… Don't access
FEA	FSR0H	-	xx	xxxx xxxx	FSR0 (Data memory pointer) high byte… Don't access
FEB	PLUSW0	-	xx	xxxx xxxx	Not physical register
FEC	PREINC0	-	xx	xxxx xxxx	Not physical register
FED	POSTDEC0	-	xx	xxxx xxxx	Not physical register
FEE	POSTINC0	-	xx	xxxx xxxx	Not physical register
FEF	INDF0	-	xx	xxxx xxxx	Not physical register
FF0	INTCON3	W	C0	1100 0000	External interrupt control… disable(default)
FF1	INTCON2	W	F5	1111 0101	External and Timer0 interrupt control… Default
FF2	INTCON	W	E0	1110 0000	Interrupt control… enable interrupts, TMR0 int enable
FF3	PRODL	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF4	PRODH	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF5	TABLAT	-	xx	xxxx xxxx	Program memory table latch… Don't access
FF6	TBLPTRL	-	xx	xxxx xxxx	Program memory table pointer low byte… Don't access
FF7	TBLPTRH	-	xx	xxxx xxxx	Program memory table pointer high byte… Don't access
FF8	TBLPTRU	-	xx	xxxx xxxx	Program memory table pointer upper byte… Don't access
FF9	PCL	-	xx	xxxx xxxx	Program counter low byte (also defined as PCLAT)… Don't access
FFA	PCLATH	-	xx	xxxx xxxx	Program counter latch low byte… Don't access
FFB	PCLATU	-	xx	xxxx xxxx	Program counter latch upper byte… Don't access
FFC	STKPTR	-	xx	xxxx xxxx	Stack pointer… Don't access
FFD	TOSL	-	xx	xxxx xxxx	Top-of-stack low byte… Don't access
FFE	TOSH	-	xx	xxxx xxxx	Top-of-stack high byte… Don't access
FFF	TOSU	-	xx	xxxx xxxx	Top-of-stack upper byte… Don't access

*1: SPBRG = ((F_{OSC} / [Baud rate]) / 16) - 1 = ((8M / 19200) / 16) – 1 ≒ 25 (19h).
*2: TMR0L = (256 - 125) – 2 = 129 (81h). Clock frequency of Timer0: f = 8[MHz] / 4 / 16 / 125 = 1000[Hz]

Source Files [v0.1]

Module	Source	Header	Description
MAIN	main.c V0.10 V0.11 V0.12	main.h V0.10 V0.11 V0.12	Not blink LED Blink LED, output status to Console Soft timer, Echo back characters received from Console
INIT	init.c V0.10 V0.11 V0.12	init.h V0.10 V0.11 V0.12	Send message to Console Tx interrupt enable Use Timer0 for soft timer
DIAG	diag.c V0.01 V0.10	diag.h V0.00 V0.10	Blink LED and relays Called by main() each time soft timer reaches zero
CNSL	cnsl.c V0.00 V0.10 V0.11	cnsl.h V0.00 V0.10	Implement putch() Utilize Tx buffer and interrupt Receive char from Console
INTR	intr.c V0.00 V0.01	-	Interrupt service routines (ISRs) Rx interrupt supported, high-priority interrupt supported

Sequence [v0.1]

Starting UART transmitter

1. Set SPBRG = 25… baud rate… 19,200 baud
2. TXSTA<4>:SYNC=0… asynchronous mode, TXSTA<2>:BRGH=1… high speed
3. INTCON<6>:GIEL=1… enable low-priority interrupt
4. RCSTA<7>:SPEN=1… Enable UART
5. TXSTA<5>:TXEN=1… Tx enable

6. PIE<4>:TXIE=1… Tx interrupt enable

Initialize Timer0
1. INTCON2<2>:TMR0IP=1… high-priority interrupt
2. TMR0L =129 (81h)… overflow every 1msec *1
3. T0CON=D3h (1101 0011b)
   <7>:TMR0ON=1… enable Timer0
   <6>:T08BIT=1… 8-bit counter
   <5>:T0CS=0… use internal clock
   <4>:T0SE=1… clock edge (default)… don't care
   <3>:PSA=0… use prescaler
   <2:0>:T0PS<2:>=011b… 1/16 prescaler
4. INTCON<5>TMR0IE=1… enable Timer0 interrupt

*1: TMR0L = (256 – t×f×p) – w = 256 – (0.001×2000000) / 16 - 2 = 129 (81h)
where
t: interval time of Timer0 interrupt… =0.001 (1msec)
f: frequency of internal instruction clock… $F_{OSC}/4$ = 8MHz/4 = 2000000[Hz]
p: prescale… 1/16
w: waiting instruction cycles before Timer0 starts… =2

Interrupts [v0.1]

High-priority: Timer0
Low-priority: UART (Console) transmit interrupt, receive interrupt

Soft Timer [v0.1]

App sets the time to wait to soft timer in msec.
Each Timer0 interrupt decrements soft timer.
Main routine checks soft timer at the beginning of the main loop.

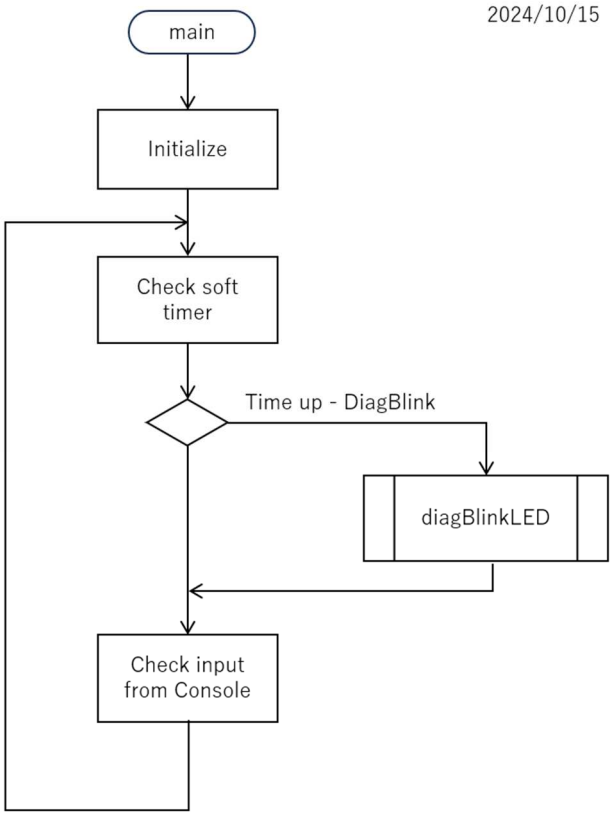
Globals [v0.1]

Variable name	Members	Implement file	Description
cnslTxBuf	FIFO buffer, counter	cnsl.c	
cnslRxBuf	FIFO buffer, counter	cnsl.c	
mainSoftTimer	16-bit counter	main.c	Counter is decremented every 1msec

Flowchart of main()

Flowchart of main() [v0.12]

2024/10/15



CC-218 FW – Flowchart of MAIN [V0.12]

Ver.0.2

Check communication with DISP board (BD1) and its basic feature.
Ver.0.20: Turn on/off every LED on BD1-2.
Ver.0.21: Read status of Rotary SW. Evoke diagnostic routine by commands from Console.

Specifications

Communicate with the display controller AS1115 (BD1:U1) via I^2C.
MCU is master, AS1115 is slave.
Baud rate: 100kHz
High-priority interrupt is used for I^2C.

Configuration of MCU [v0.2]

Internal OSC used, WDT disabled and single-supply ICSP disabled.
Same as Ver.0.1.

SFR settings [v0.2]

Address	Name	R/W	Hex	Binary	Description
F80	PORTA	R	00	0000 0000	Status of Port A pins. Always 00h because Port A is disabled.

F81	PORTB	R	00	0000 0000	Status of Port B pins. Always 00h because Port B is disabled.
F82	PORTC	R	x0	00x0 0000	Status of Port C pins. Bit 5 is controlled by F/W. The other bits are always '0'
F84	PORTE	R	00	0000 0000	Status of Port E pins. Always 00h because Port E is disabled.
F89	LATA	R/W	00	0000 0000	Latch for Port A. Unused (default).
F8A	LATB	R/W	0X	0000 0x00	Latch for Port B. Alternate RB2 output.
F8B	LATC	R/W	x0	00x0 0000	Latch for Port C. RC5 is used to blink LED.
F92	TRISA	W	FF	1111 1111	All output buffers in tri-state (this port is input)(default).
F93	TRISB	W	FB	1111 1011	All output buffers but RB2 in tri-state (RB2 is output)
F94	TRISC	W	DF	1101 1111	All output buffers but RC5 in tri-state (RC5 is output).
F9B	OSCTUNE	W	00	0000 0000	Default
F9D	PIE1	W	38	0011 1000	Rx/Tx int enable, MCCP (I2C) int enable
F9E	PIR1	R	00	0000 0000	Peripheral interrupt request flag
F9F	IPR1	W	CF	1100 1111	Peripheral interrupt priority… UART in low priority
FA0	PIE2	W	00	0000 0000	All peripheral interrupts inhibited… Default
FA1	PIR2	R	00	0000 0000	Peripheral interrupt request flag
FA2	IPR2	W	FF	1111 1111	Peripheral interrupt priority… Default
FA6	EECON1	-	xx	xxxx xxxx	EEPROM control… Don't access
FA7	EECON2	-	xx	xxxx xxxx	EEPROM control… Don't access
FA8	EEDATA	-	xx	xxxx xxxx	EEPROM data… Don't access
FA9	EEADR	-	xx	xxxx xxxx	EEPROM address… Don't access
FAB	RCSTA	W	90	1001 0000	Serial port receive status and control… Serial port enable
FAC	TXSTA	W	26	0010 0110	Serial port transmit status and control… Transmit disable Bit-5 (TXEN) is set after related registers are initialized)
FAD	TXREG	W	xx	xxxx xxxx	EUSART transmit register
FAE	RCREG	R	xx	xxxx xxxx	EUSART receive register
FAF	SPBRG	W	19	0001 1001	Serial port baud rate generator… 19,200bps
FB0	SPBRGH	-	xx	xxxx xxxx	Serial port baud rate generator high byte… Don't access
FB1	T3CON	W	00	0000 0000	Timer control… default
FB2	TMR3L	-	xx	xxxx xxxx	Timer3 register low byte… Don't access
FB3	TMR3H	-	xx	xxxx xxxx	Timer3 register high byte… Don't access
FB4	CMCON	W	07	0000 0111	Comparator control… Default
FB5	CVRCON	W	00	0000 0000	Comparator voltage reference… Default
FB6	ECCP1AS	W	00	0000 0000	ECCP auto-shutdown control… Default
FB7	PWM1CON	W	00	0000 0000	PWM dead-band delay… Default
FB8	BAUDCON	W	02	0000 0010	Baud rate control… Enable receive wake-up
FBA	CCP2CON	-	xx	xxxx xxxx	CCP2 control… Don't access
FBB	CCPR2L	-	xx	xxxx xxxx	Capture/compare/PWM register 2 low byte… Don't access
FBC	CCPR2H	-	xx	xxxx xxxx	Capture/compare/PWM register 2 high byte… Don't access
FBD	CCP1CON	-	xx	xxxx xxxx	CCP1 control… Don't access
FBE	CCPR1L	-	xx	xxxx xxxx	Capture/compare/PWM register 1 low byte… Don't access
FBF	CCPR1H	-	xx	xxxx xxxx	Capture/compare/PWM register 1 high byte… Don't access
FC0	ADCON2	W	00	0000 0000	A/D control 2
FC1	ADCON1	W	00	0000 0000	A/D control 1
FC2	ADCON0	W	00	0000 0000	A/D control 0
FC3	ADRESL	-	xx	xxxx xxxx	A/D result low byte… Don't access
FC4	ADRESH	-	xx	xxxx xxxx	A/D result high byte… Don't access
FC5	SSPCON2	R/W	xx	0xxx xxxx	MSSP control 2… control Tx/Rx during communication
FC6	SSPCON1	R/W	28	0010 1000	MSSP control 1… Enabled as I^2C Master Mode
FC7	SSPSTAT	R/W	80	1000 0000	MSSP status (I^2C)… Standard speed (100kHz)
FC8	SSPADD	W	13	0001 0011	MSSP clock frequency… 100kHz *1
FC9	SSPBUF	R/W	xx	xxxx xxxx	MSSP Receive/Transmit buffer
FCA	T2CON	W	00	0000 0000	Timer2 control… Default (disable)
FCB	PR2	-	xx	xxxx xxxx	Timer2 period… Don't access
FCC	TMR2	-	xx	xxxx xxxx	Timer2… Don't access
FCD	T1CON	W	00	0000 0000	Timer1 control… Default (disable)
FCE	TMR1L	-	xx	xxxx xxxx	Timer1 low byte… Don't access

FCF	TMR1H	-	xx	xxxx xxxx	Timer1 high byte… Don't access
FD0	RCON	W	DF	1101 1111	Reset control… Enable interrupt priority level
FD1	WDTCON	W	00	0000 0000	Watch dog timer control… Default (disable)
FD2	HLVDCON	W	05	0000 0101	High/low voltage detect control… Default (disable)
FD3	OSCCON	R/W	72	0111 0010	Oscillator control… Internal oscillator, 8MHz
FD5	TOCON	W	C3	1100 0011	Timer0 control… Enable, 8-bit, 1/16 prescale
FD6	TMR0L	W	81	1000 0011	Timer0 low byte… 1msec interval
FD7	TMR0H	-	xx	xxxx xxxx	Timer0 high byte… Don't access
FD8	STATUS	R	xx	xxxx xxxx	Status… Don't access
FD9	FSR2L	-	xx	xxxx xxxx	FSR2 (Data memory pointer) low byte… Don't access
FDA	FSR2H	-	xx	xxxx xxxx	FSR2 (Data memory pointer) high byte… Don't access
FDB	PLUSW2	-	xx	xxxx xxxx	Not physical register
FDC	PREINC2	-	xx	xxxx xxxx	Not physical register
FDD	POSTDEC2	-	xx	xxxx xxxx	Not physical register
FDE	POSTINC2	-	xx	xxxx xxxx	Not physical register
FDF	INDF2	-	xx	xxxx xxxx	Not physical register
FE0	BSR	-	xx	xxxx xxxx	Bank select… Don't access
FE1	FSR1L	-	xx	xxxx xxxx	FSR1 (Data memory pointer) low byte… Don't access
FE2	FSR1H	-	xx	xxxx xxxx	FSR1 (Data memory pointer) high byte… Don't access
FE3	PLUSW1	-	xx	xxxx xxxx	Not physical register
FE4	PREINC1	-	xx	xxxx xxxx	Not physical register
FE5	POSTDEC1	-	xx	xxxx xxxx	Not physical register
FE6	POSTINC1	-	xx	xxxx xxxx	Not physical register
FE7	INDF1	-	xx	xxxx xxxx	Not physical register
FE8	WREG	-	xx	xxxx xxxx	Working register… Don't access
FE9	FSR0L	-	xx	xxxx xxxx	FSR0 (Data memory pointer) low byte… Don't access
FEA	FSR0H	-	xx	xxxx xxxx	FSR0 (Data memory pointer) high byte… Don't access
FEB	PLUSW0	-	xx	xxxx xxxx	Not physical register
FEC	PREINC0	-	xx	xxxx xxxx	Not physical register
FED	POSTDEC0	-	xx	xxxx xxxx	Not physical register
FEE	POSTINC0	-	xx	xxxx xxxx	Not physical register
FEF	INDF0	-	xx	xxxx xxxx	Not physical register
FF0	INTCON3	W	C0	1100 0000	External interrupt control… disable(default)
FF1	INTCON2	W	F5	1111 0101	External and Timer0 interrupt control… Default
FF2	INTCON	W	E0	1110 0000	Interrupt control… enable interrupts, TMR0 int enable
FF3	PRODL	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF4	PRODH	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF5	TABLAT	-	xx	xxxx xxxx	Program memory table latch… Don't access
FF6	TBLPTRL	-	xx	xxxx xxxx	Program memory table pointer low byte… Don't access
FF7	TBLPTRH	-	xx	xxxx xxxx	Program memory table pointer high byte… Don't access
FF8	TBLPTRU	-	xx	xxxx xxxx	Program memory table pointer upper byte… Don't access
FF9	PCL	-	xx	xxxx xxxx	Program counter low byte (also defined as PCLAT)… Don't access
FFA	PCLATH	-	xx	xxxx xxxx	Program counter latch low byte… Don't access
FFB	PCLATU	-	xx	xxxx xxxx	Program counter latch upper byte… Don't access
FFC	STKPTR	-	xx	xxxx xxxx	Stack pointer… Don't access
FFD	TOSL	-	xx	xxxx xxxx	Top-of-stack low byte… Don't access
FFE	TOSH	-	xx	xxxx xxxx	Top-of-stack high byte… Don't access
FFF	TOSU	-	xx	xxxx xxxx	Top-of-stack upper byte… Don't access

*1: SSPADD = F_{OSC} / (4 × c) – 1 = 8MHz / (4 × 100kHz) = 19 (13h)
where c = [I^2C clock frequency] = 100kHz

Source files [v0.2]

Module	Source	Header	Description

MAIN	main.c V0.20 V0.21	main.h V0.20 V0.21	Control DISP module: 7-seg LED display Operation modes changeable by commands
INIT	init.c V0.20	init.h V0.20	Initialize DIAG and DISP modules
DIAG	diag.c V0.20 V0.21	diag.h V0.20 V0.21	7-seg LED test, demo display Test selectable by commands
CNSL	cnsl.c V0.11 V0.12	cnsl.h V0.10 V0.11	Transmit texts and receive characters to/from Console Some drivers including getch() added
INTR	intr.c V0.02 V0.03	-	I2C communication supported Soft timers supported
DISP	disp.c V0.00 V0.10	disp.h V0.00 V0.10	Control BD3 (CC-218 DISP) to display numeric characters More useful service routines added

Settings of AS1115

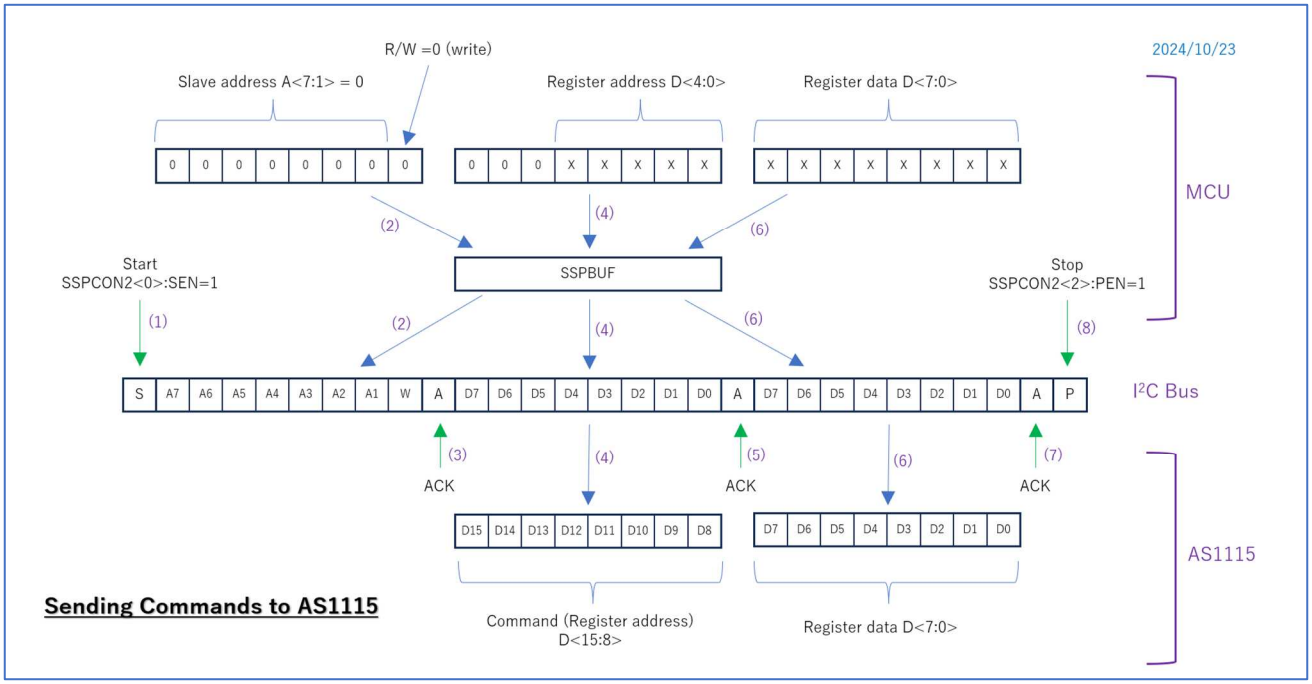
Slave address of AS1115: 0
Decode: disable
Number of digits: 3 (Dig-0 ~ Dig-2)
Intensity: half (subject to change after the visual check)

Control register settings

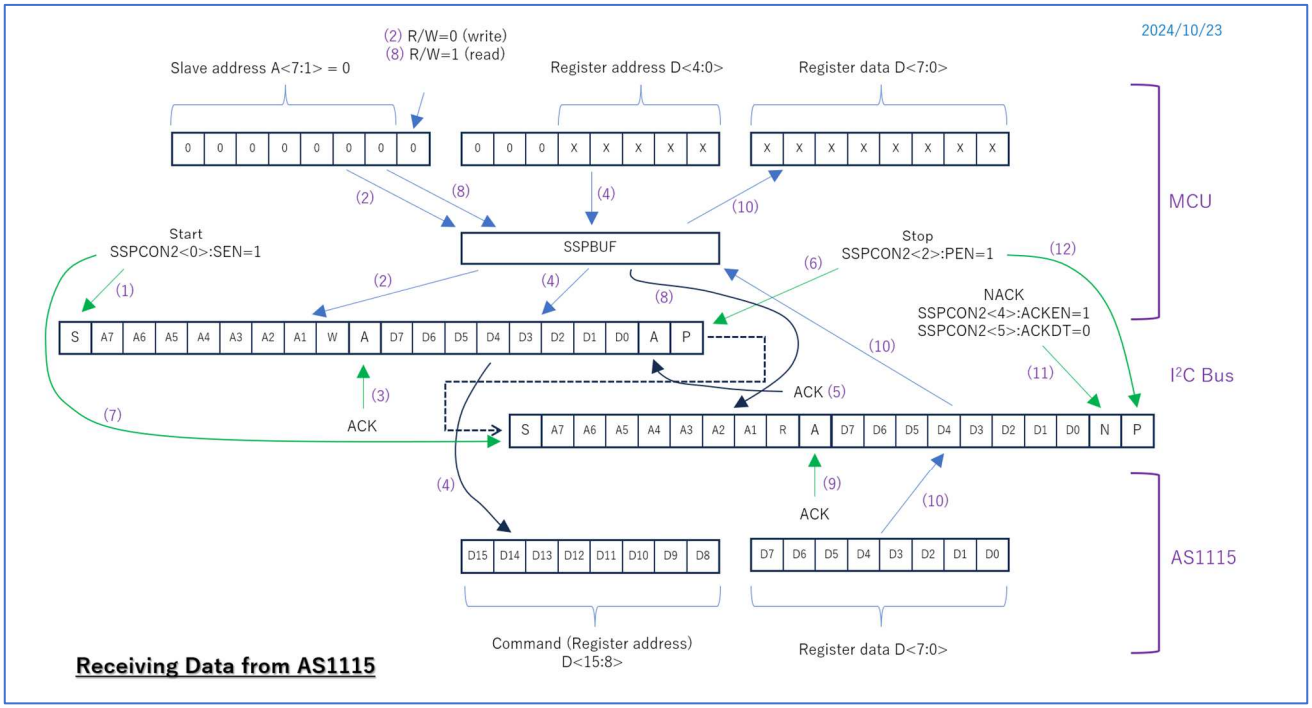
Name	Address	Read/Write	Value	Description
Data Dig<0>	00h	W	xxh	Segment data of Dig-0
Data Dig<1>	01h	W	xxh	Segment data of Dig-1
Data Dig<2>	02h	W	xxh	Segment data of Dig-2
Decode-mode	09h	W	00h	No-decode
Global Intensity	0Ah	W	07h	Half intensity
Scan Limit	0Bh	W	02h	Dig-<0:2>
Shutdown	0Ch	-	-	Don't use in V0.2
I^2C Self Addressing	2Dh	-	-	Don't care
Feature	0Eh	W	00h	(default)
Display Test Mode	0Fh	W	00h 02h 04h	Normal mode LED short test LED open test
Intensity Dig-<0:1>	10h	W	-	Don't care
Intensity Dig-<2:3>	11h	W	-	Don't care
Intensity Dig-<4:5>	12h	W	-	Don't care
Intensity Dig-<6:7>	13h	W	-	Don't care
Diagnostics Dig-0	14h	R	xxh	Result of diagnostics
Diagnostics Dig-1	15h	R	xxh	Result of diagnostics
Diagnostics Dig-2	16h	R	xxh	Result of diagnostics
Diagnostics Dig-3	17h	R	xxh	Don't care
Diagnostics Dig-4	18h	R	xxh	Don't care
Diagnostics Dig-5	19h	R	xxh	Don't care
Diagnostics Dig-6	1Ah	R	xxh	Don't care
Diagnostics Dig-7	1Bh	R	xxh	Don't care
KEYA	1Ch	R	xxh	Don't care
KEYB	1Dh	R	Bit-6: SW_PHONO Bit-5: SW_DAC Bit-4: SW_AUX	Reading of SW2 (Rotary SW)

Note: Registers that are not used in this application are omitted in this table.

Sending commands to AS1115



Receiving data from AS1115



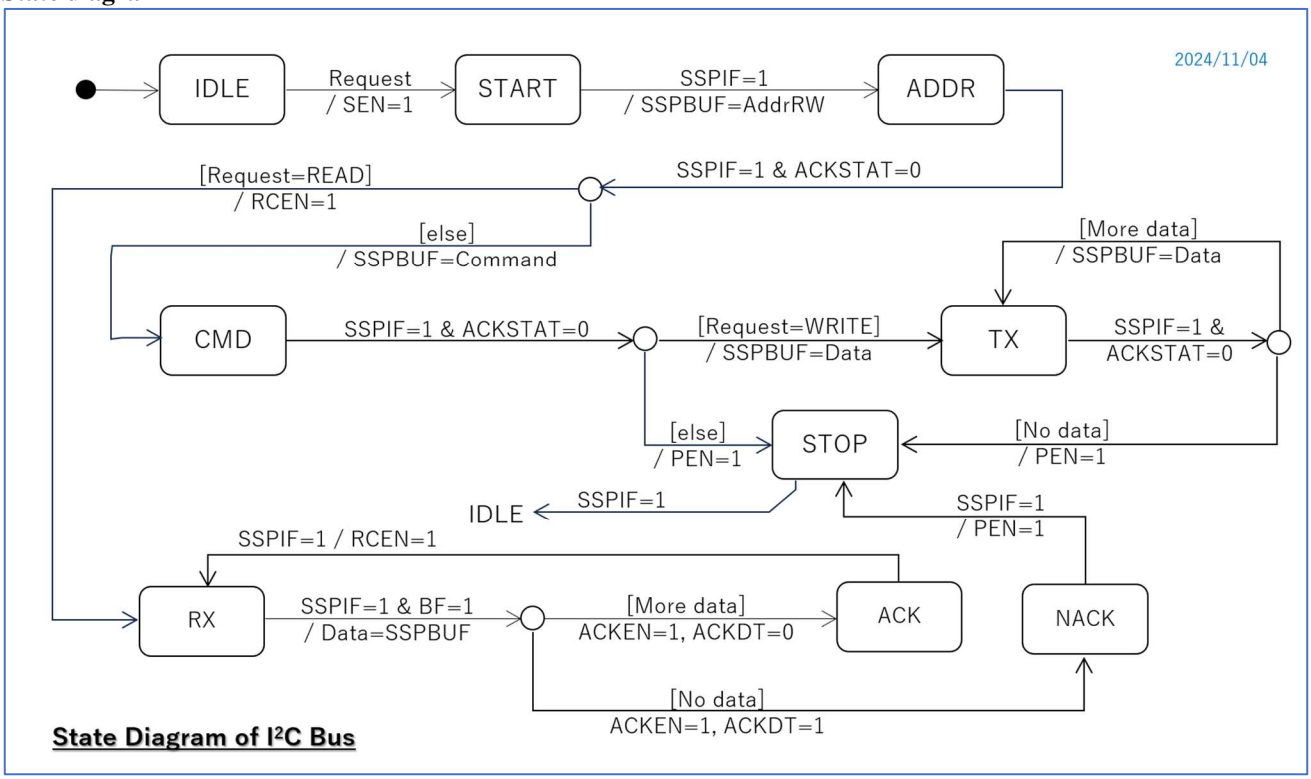
I²C State Machine

State table

State	Previous State	Entry	Do	Exit	Note
IDLE	(initial) STOP	 SSPIF=1	(none)	Tx/Rx Request	Tx/Rx Request: Called by another module
START	IDLE	Tx/Rx Request	SEN=1	SSPIF=1	

ADDR	START	SSPIF=1	SSPBUF= AddrRW	SSPIF=1	AddrRW: <7:1>=0, <0>=RW RW is set by caller: RW=1: read, RW=0: write
CMD	ADDR	SSPIF=1 & ACKSTAT=0 & Request=!READ	SSPBUF=Command	SSPIF=1	Command: Register address
TX	CMD	SSPIF=1 & ACKSTAT=0 & Request=WRITE	SSPBUF=Data	SSPIF=1	Data: Register data to be sent
	TX	SSPIF=1 & ACKSTAT=0 & [More data]			
STOP	CMD	SSPIF=1 & ACKSTAT=0 & Request=CMD	PEN=1	SSPIF=1	
	TX	SSPIF=1 & ACKSTAT=0 & [No data]			
	NACK	SSPIF=1			
RX	ADDR	SSPIF=1 & ACKSTAT=0 & Request=READ	RCEN=1	SSPIF=1	
	ACK	SSPIF=1			
ACK	RX	SSPIF=1 & BF=1 & [More data]	Data=SSPBUF ACKEN=1 ACKDT=0	SSPIF=1	Data: Received register data Send ACK
NACK	RX	SSPIF=1 & BF=1 & [No data]	Data=SSPBUF ACKEN=1 ACKDT=1	SSPIF=1	Data: Received register data Send NACK

State diagram



Data Structure of DISP

Transmission/Reception

Struct	Member	Bitwise	Description

dispCtrlData	BYTE AddrRW	<7:1>: Addr (always 0) <0>: RW… RW=1: Read, RW=0: Write	I^2C slave address Read/Write
	BYTE Command		AS1115 register address
	BYTE Data	(see Segment Data)	AS1115 register data
	BYTE Request		Read/Write/Command
	BYTE State		State code
	BYTE Status		Status code
	BYTE Bytes		Number of bytes

BYTE: unsigned char

Segment data

Bit	7	6	5	4	3	2	1	0
Segment	dp	a	b	c	d	e	f	g

Character data

Character	B7:dp	B6:a	B5:b	B4:c	B3:d	B2:e	B1:f	B0:g	Hex
0	X	1	1	1	1	1	1	0	7E/FE
1	X	0	1	1	0	0	0	0	30/B0
2	X	1	1	0	1	1	0	1	6D/ED
3	X	1	1	1	1	0	0	1	79/F9
4	X	0	1	1	0	0	1	1	33/B3
5	X	1	0	1	1	0	1	1	5B/DB
6	X	1	0	1	1	1	1	1	5F/DF
7	X	1	1	1	0	0	0	0	70/F0
8	X	1	1	1	1	1	1	1	7F/FF
9	X	1	1	1	1	0	1	1	7B/FB
-	X	0	0	0	0	0	0	1	01/81

Data structure of DIAG

Diagnostics number

Test	Number	Description
No test	0	No test executed
Blink	1	Blink LED of RC5 (BD3:U1:P16)
Open	2	7-seg LEDs (BD1:LED1-3, BD2:LED1-3) open test
Short	3	7-seg LEDs (BD1:LED1-3, BD2:LED1-3) short test
Demo	4	7-seg LEDs (BD1:LED1-3, BD2:LED1-3) demonstration display
Visual	5	7-seg LEDs (BD1:LED1-3, BD2:LED1-3) visual check

State table of DIAG

State	Previous State	Entry	Do	Exit	Note
IDLE	(initial)		(none)	Start Request	
	DIAG_BLINK DIAG_OPEN DIAF_SHORT DIAG_DEMO	Stop Request Diag=1~4			
DIAG_BLINK	IDLE	Start Request & Diag=1	Entry: Start blinking LED Exit: Stop blinking LED	Stop Request & Diag=1	
DIAG_OPEN	IDLE	Start Request & Diag=2	Send open test command to DISP	Result of Dig-0 returned from DISP	
DIAG_SHORT	IDLE	Start Request & Diag=3	Send short test command to DISP	Result returned from DISP	
DIAG_DEMO	IDLE	Start Request & Diag=4	Send test pattern to DISP	Stop Request & Diag=4	

Control variables

Struct	Member	Bitwise	Description
diagCtrlData	BYTE TestNum		Test number
	BYTE TestStatus		Status code
	BYTE TestResult[3]		Test result for each digit
	BYTE State		State

Data structure of MAIN

State

State	Number	Description
ALONE	0	CC-218 has no slave device
DIAG	1	CC-218 executes (a) test routine(s)
MASTER	2	CC-218 functions as Master device

Ver.0.3

Add PWM and ADC features to establish volume control.
Ver.0.30: Enable PWM and output 10kHz square wave to VR1 (1kohm variable resistor).
Ver.0.31: Enable ADC and read voltage of VR1.
Ver.0.32: Calculate gain data to be set to eVolume chip PGA3210, and display actual gain on CC-218 DISP.

Specifications

Output of PWM: 10kHz square wave with duty ratio=50%.
PWM module: CCP1
~~Low-priority interrupt is used for ADC.~~ ➔ Interrupt is not used, because reading VR1 doesn't need quick response.
VR1 data is smoothed to eliminate chattering.

Configuration of MCU [v0.3]

Internal OSC used, WDT disabled and single-supply ICSP disabled.
Same as Ver.0.1.

SFR settings [v0.3]

Address	Name	R/W	Hex	Binary	Description
F80	PORTA	R	00	0000 0000	Status of Port A pins. Always 00h because Port A is disabled.
F81	PORTB	R	00	0000 0000	Status of Port B pins. Always 00h because Port B is disabled.
F82	PORTC	R	x0	00x0 0000	Status of Port C pins. Bit-5 is controlled by F/W. The other bits are always '0'
F84	PORTE	R	00	0000 0000	Status of Port E pins. Always 00h because Port E is disabled.
F89	LATA	R/W	00	0000 0000	Latch for Port A. Unused (default).
F8A	LATB	R/W	0X	0000 0x00	Latch for Port B. Alternate RB2 output.
F8B	LATC	R/W	x0	00x0 0000	Latch for Port C. RC5 is used to blink LED.
F92	TRISA	W	FF	1111 1111	All output buffers in tri-state (this port is input)(default).
F93	TRISB	W	FB	1111 1011	All output buffers but RB2 in tri-state (RB2 is output)
F94	TRISC	W	DF	1101 1111	All output buffers but RC5 in tri-state (RC5 is output).
F9B	OSCTUNE	W	00	0000 0000	Default
F9D	PIE1	W	38	0011 1000	Rx/Tx int enable, MCCP (I2C) int enable
F9E	PIR1	R	00	0000 0000	Peripheral interrupt request flag
F9F	IPR1	W	CF	1100 1111	Peripheral interrupt priority… UART in low priority

FA0	PIE2	W	00	0000 0000	All peripheral interrupts inhibited… Default
FA1	PIR2	R	00	0000 0000	Peripheral interrupt request flag
FA2	IPR2	W	FF	1111 1111	Peripheral interrupt priority… Default
FA6	EECON1	-	xx	xxxx xxxx	EEPROM control… Don't access
FA7	EECON2	-	xx	xxxx xxxx	EEPROM control… Don't access
FA8	EEDATA	-	xx	xxxx xxxx	EEPROM data… Don't access
FA9	EEADR	-	xx	xxxx xxxx	EEPROM address… Don't access
FAB	RCSTA	W	90	1001 0000	Serial port receive status and control… Serial port enable
FAC	TXSTA	W	26	0010 0110	Serial port transmit status and control… Transmit disable Bit-5 (TXEN) is set after related registers are initialized)
FAD	TXREG	W	xx	xxxx xxxx	EUSART transmit register
FAE	RCREG	R	xx	xxxx xxxx	EUSART receive register
FAF	SPBRG	W	19	0001 1001	Serial port baud rate generator… 19,200bps
FB0	SPBRGH	-	xx	xxxx xxxx	Serial port baud rate generator high byte… Don't access
FB1	T3CON	W	00	0000 0000	Timer control… default
FB2	TMR3L	-	xx	xxxx xxxx	Timer3 register low byte… Don't access
FB3	TMR3H	-	xx	xxxx xxxx	Timer3 register high byte… Don't access
FB4	CMCON	W	07	0000 0111	Comparator control… Default
FB5	CVRCON	W	00	0000 0000	Comparator voltage reference… Default
FB6	ECCP1AS	W	00	0000 0000	ECCP auto-shutdown control… Default
FB7	PWM1CON	W	00	0000 0000	PWM dead-band delay… Default
FB8	BAUDCON	W	02	0000 0010	Baud rate control… Enable receive wake-up
FBA	CCP2CON	-	xx	xxxx xxxx	CCP2 control… Don't access
FBB	CCPR2L	-	xx	xxxx xxxx	Capture/compare/PWM register 2 low byte… Don't access
FBC	CCPR2H	-	xx	xxxx xxxx	Capture/compare/PWM register 2 high byte… Don't access
FBD	CCP1CON	W	0C	0000 1100	CCP1 control… PWM mode, LSBs of duty cycle (Set after T2CON) *2
FBE	CCPR1L	W	64	0110 0100	Capture/compare/PWM register 1 low byte… MSBs of duty cycle *2
FBF	CCPR1H	-	xx	xxxx xxxx	Capture/compare/PWM register 1 high byte… Don't access
FC0	ADCON2	W	21	0010 0001	A/D control 2… T_{ACQ}=8*T_{AD}, Clock=F_{OSC}/8
FC1	ADCON1	W	0E	0000 1110	A/D control 1… Port configuration (AN0 only)
FC2	ADCON0	W	0x	0000 00xx	A/D control 0… <1:0> are set in driver
FC3	ADRESL	-	xx	xxxx xxxx	A/D result low byte… Don't access
FC4	ADRESH	-	xx	xxxx xxxx	A/D result high byte… Don't access
FC5	SSPCON2	R/W	xx	0xxx xxxx	MSSP control 2… control Tx/Rx during communication
FC6	SSPCON1	R/W	28	0010 1000	MSSP control 1… Enabled as I^2C Master Mode
FC7	SSPSTAT	R/W	80	1000 0000	MSSP status (I^2C)… Standard speed (100kHz)
FC8	SSPADD	W	13	0001 0011	MSSP clock frequency… 100kHz
FC9	SSPBUF	R/W	xx	xxxx xxxx	MSSP Receive/Transmit buffer
FCA	T2CON	W	04	0000 0100	Timer2 control… Enabled, prescale=1:1 (Set after PR2, CCPR1L)
FCB	PR2	W	C8	1100 1000	Timer2 period… =200, 100[usec], 10[kHz] *1
FCC	TMR2	-	xx	xxxx xxxx	Timer2… Don't access
FCD	T1CON	W	00	0000 0000	Timer1 control… Default (disable)
FCE	TMR1L	-	xx	xxxx xxxx	Timer1 low byte… Don't access
FCF	TMR1H	-	xx	xxxx xxxx	Timer1 high byte… Don't access
FD0	RCON	W	DF	1101 1111	Reset control… Enable interrupt priority level
FD1	WDTCON	W	00	0000 0000	Watch dog timer control… Default (disable)
FD2	HLVDCON	W	05	0000 0101	High/low voltage detect control… Default (disable)
FD3	OSCCON	R/W	72	0111 0010	Oscillator control… Internal oscillator, 8MHz
FD5	T0CON	W	C3	1100 0011	Timer0 control… Enable, 8-bit, 1/16 prescale
FD6	TMR0L	W	81	1000 0011	Timer0 low byte… 1msec interval
FD7	TMR0H	-	xx	xxxx xxxx	Timer0 high byte… Don't access
FD8	STATUS	R	xx	xxxx xxxx	Status… Don't access
FD9	FSR2L	-	xx	xxxx xxxx	FSR2 (Data memory pointer) low byte… Don't access
FDA	FSR2H	-	xx	xxxx xxxx	FSR2 (Data memory pointer) high byte… Don't access
FDB	PLUSW2	-	xx	xxxx xxxx	Not physical register
FDC	PREINC2	-	xx	xxxx xxxx	Not physical register

FDD	POSTDEC2	-	xx	xxxx xxxx	Not physical register
FDE	POSTINC2	-	xx	xxxx xxxx	Not physical register
FDF	INDF2	-	xx	xxxx xxxx	Not physical register
FE0	BSR	-	xx	xxxx xxxx	Bank select… Don't access
FE1	FSR1L	-	xx	xxxx xxxx	FSR1 (Data memory pointer) low byte… Don't access
FE2	FSR1H	-	xx	xxxx xxxx	FSR1 (Data memory pointer) high byte… Don't access
FE3	PLUSW1	-	xx	xxxx xxxx	Not physical register
FE4	PREINC1	-	xx	xxxx xxxx	Not physical register
FE5	POSTDEC1	-	xx	xxxx xxxx	Not physical register
FE6	POSTINC1	-	xx	xxxx xxxx	Not physical register
FE7	INDF1	-	xx	xxxx xxxx	Not physical register
FE8	WREG	-	xx	xxxx xxxx	Working register… Don't access
FE9	FSR0L	-	xx	xxxx xxxx	FSR0 (Data memory pointer) low byte… Don't access
FEA	FSR0H	-	xx	xxxx xxxx	FSR0 (Data memory pointer) high byte… Don't access
FEB	PLUSW0	-	xx	xxxx xxxx	Not physical register
FEC	PREINC0	-	xx	xxxx xxxx	Not physical register
FED	POSTDEC0	-	xx	xxxx xxxx	Not physical register
FEE	POSTINC0	-	xx	xxxx xxxx	Not physical register
FEF	INDF0	-	xx	xxxx xxxx	Not physical register
FF0	INTCON3	W	C0	1100 0000	External interrupt control… disable(default)
FF1	INTCON2	W	F5	1111 0101	External and Timer0 interrupt control… Default
FF2	INTCON	W	E0	1110 0000	Interrupt control… enable interrupts, TMR0 int enable
FF3	PRODL	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF4	PRODH	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF5	TABLAT	-	xx	xxxx xxxx	Program memory table latch… Don't access
FF6	TBLPTRL	-	xx	xxxx xxxx	Program memory table pointer low byte… Don't access
FF7	TBLPTRH	-	xx	xxxx xxxx	Program memory table pointer high byte… Don't access
FF8	TBLPTRU	-	xx	xxxx xxxx	Program memory table pointer upper byte… Don't access
FF9	PCL	-	xx	xxxx xxxx	Program counter low byte (also defined as PCLAT)… Don't access
FFA	PCLATH	-	xx	xxxx xxxx	Program counter latch low byte… Don't access
FFB	PCLATU	-	xx	xxxx xxxx	Program counter latch upper byte… Don't access
FFC	STKPTR	-	xx	xxxx xxxx	Stack pointer… Don't access
FFD	TOSL	-	xx	xxxx xxxx	Top-of-stack low byte… Don't access
FFE	TOSH	-	xx	xxxx xxxx	Top-of-stack high byte… Don't access
FFF	TOSU	-	xx	xxxx xxxx	Top-of-stack upper byte… Don't access

*1: The frequency of square wave: 10[kHz] ➔ The period, P=100[usec]
PR2 = P / (4 * T * PS) = 100 / (4 * 0.125 * 1) = 200 (C8h)
where T is period of CPU clock; T = 1 / 8[MHz] = 0.125[usec]; PS is prescale: 1:1
*2: The period of high level, H, is determined by CCPR1L:CCP1CON<5:4> (10-bit data); H=50[usec] (50% duty)
Assume D = (CCPR1L:CCP1CON<5:4>)
D = H / (T * PS) = 50 / (0.125 * 1) = 400 (190h, 0110010000b)
where T is period of CPU clock: T = 1 / 8[MHz] = 0.125[usec]; PS is prescale: 1:1
CCPR1L = 01100100b = 64h, CCP1CON<5:4> = 00b

Source files [v0.3]

Module	Source	Header	Description
MAIN	main.c V0.30 V0.31 V0.32	main.h V0.30 V0.31 V0.32	VOLM module and I/F of VR1 added Read VR1 and display the acquired data Calculate data for PGA3210 and the gain
INIT	init.c V0.30 V0.31	init.h V0.30 V0.31	Initialize VOLM module Utilize ADC
DIAG	diag.c V0.21 V0.30	diag.h V0.21 V0.30	Tests selectable by commands Display result of ADC
CNSL	cnsl.c V0.12	cnsl.h V0.11	Device drivers for other modules

INTR	intr.c V0.03	-	I2C communication and soft timers supported
DISP	disp.c V0.10	disp.h V0.10	Device drivers for other modules
VOLM	volm.c V0.00 V0.10 V0.11	volm.h V0.00 V0.10 V0.11	Generate 10kHz square wave using PWM Read the value of VR1 using ADC Calculate gain data to be set to PGA2310 and the actual gain

Sequence

Setting PWM

1. Set the period of square wave: PR2=200(C8h)
2. Set the period of high level: CCPR1L=64h
3. Start Timer2: T2CON=04h
4. Start PWM: CCP1CON=0Ch

Setting ADC

1. Set V_{REF} and port configuration: ADCON1=0Eh
2. Select input channel AN0: ADCON0<5:2>=0h
3. Set T_{ACQ} (8*T_{AD}), A/D clock (F_{OSC}/8): ACCON2=21h
4. Enable ADC: ADCON0<0>=1
5. Start A/D: ADCON0<1>=1

Data Structure

Main

Struct	Member	Bitwise	Description
mainCtrlData	BYTE State		State
	BYTE PreviousState		Previous state
	BYTE Select	<6>:PHONO, <5>:DAC, <4>:AUX	Selected source
	BYTE GainData		Value to be set to PGA2310, ch-L
	int Offset		GainData+Offset → ch-R

- BYTE: unsigned char, WORD: unsigned short

Linearity of VR_IN

First measurement

Position of KB1	Voltage at WIPER V_W [mV_{p-p}]	Voltage at VR_IN V_{IN}[mV_{DC}]	V_{IN} / V_W
7 (min)	13.12	91.29	6.95
8	351	160.5	0.457
9	859.1	390.8	0.455
10	1549	705.5	0.455
11	1967	893.5	0.454
12	2553	1162	0.443
1	3278	1496	0.456
2	3825	1739	0.455
3	4323	1969	0.455
4	4922	3777	0.767
5 (max)	5145	3846	0.748

Some adjustment is required.

Settings of PGA2310 eVolume chip

The gain G is calculated by the following equation:

G = 31.5 – [0.5 * (255 – N)]

where N is the value to be set to PGA2310, whose range is 1~255.

N is calculated by the following equation:

N = 192 + 2G
Max gain G_{max} is specified to be +3dB. N for G_{max} is:
N = 192 + 2 * 3 = 198
N is stipulated to be an even number.
2, 4, 6, …, 198 (99 steps)
N = 0 makes mute the signal (the output of PGA2310 is grounded)

For the minimum value obtained from ADC (V_{min}), N = 0.
For the maximum value obtained from ADC (V_{max}), N = 198.
$N = 198 * (V_{in} - V_{min}) / (V_{max} - V_{min})$

Gain Data (N) Calculation

VR_IN_{max} = 2100[mV] ➔ D_{max} = 27,000
VR_IN_{min} = 100[mV] ➔ D_{min} = 1,000

Max gain: N = 198 (G_{max}=+3dB)
Min gain: ~~N = 2 (-94.5dB)~~ N=72 (G_{min}=-60dB)
(N is always even number)

Equation:
~~$N = 198 * (D - D_{min}) / (D_{max} - D_{min}) = 198 * (D - 1000) / 26000$~~
$N = (G_{max} - G_{min}) * (D - D_{min}) / (D_{max} - D_{min}) + G_{min} = 126 * (D - 1000) / 26000 + 72$

When D < 1,000, N = 0 (mute)

Ver.0.4

Send gain data to eVolume chip PGA2310, and drive relays of selector.
In this version, CC-218 can be used as a preamp. ➔ It can be used for listening trials.
Ver.0.40: Send gain data to eVolume chip PGA3210 to control the gain.

Specifications

Control gain in the range of mute (-∞dB), -60dB ~ +3dB by 1dB step
Select source (drive relays, BD4:RL1-6) according to the reading of SW2 (rotary switch)

Configuration of MCU [v0.4]

Internal OSC used, WDT disabled and single-supply ICSP disabled.
Same as Ver.0.1.

SFR settings [v.0.4]

Address	Name	R/W	Hex	Binary	Description
F80	PORTA	R	xx	1x0x xxx0	Status of Port A… Used for I/F w/ PGA2310 (BD4:U7)
F81	PORTB	R	0x	0000 0xxx	Status of Port B… Used for relays (BD4:RL1-6)
F82	PORTC	R	x0	00x0 0000	Status of Port C… RC5 is controlled by F/W. The other bits are always '0'
F84	PORTE	R	00	0000 0000	Status of Port E pins. Always 00h because Port E is disabled
F89	LATA	R/W	4E	0100 1110	Latch for Port A… Initial state of I/F w/ PGA2310
F8A	LATB	R/W	0X	0000 0xxx	Latch for Port B… Used for relays (BD4:RL1-6)
F8B	LATC	R/W	x0	00x0 0000	Latch for Port C… RC5 is used to blink LED
F92	TRISA	W	A1	1010 0001	Tristate control for Port A… RA1-4,6 are outputs
F93	TRISB	W	FB	1111 1000	Tristate control for Port B… RB0-2 are outputs
F94	TRISC	W	DB	1101 1011	Tristate control for Port C… RC2,5 are output
F9B	OSCTUNE	W	00	0000 0000	Default

F9D	PIE1	W	38	0011 1000	Rx/Tx int enable, MCCP (I2C) int enable
F9E	PIR1	R	00	0000 0000	Peripheral interrupt request flag
F9F	IPR1	W	CF	1100 1111	Peripheral interrupt priority… UART in low priority
FA0	PIE2	W	00	0000 0000	All peripheral interrupts inhibited… Default
FA1	PIR2	R	00	0000 0000	Peripheral interrupt request flag
FA2	IPR2	W	FF	1111 1111	Peripheral interrupt priority… Default
FA6	EECON1	-	xx	xxxx xxxx	EEPROM control… Don't access
FA7	EECON2	-	xx	xxxx xxxx	EEPROM control… Don't access
FA8	EEDATA	-	xx	xxxx xxxx	EEPROM data… Don't access
FA9	EEADR	-	xx	xxxx xxxx	EEPROM address… Don't access
FAB	RCSTA	W	90	1001 0000	Serial port receive status and control… Serial port enable
FAC	TXSTA	W	26	0010 0110	Serial port transmit status and control… Transmit disable Bit-5 (TXEN) is set after related registers are initialized)
FAD	TXREG	W	xx	xxxx xxxx	EUSART transmit register
FAE	RCREG	R	xx	xxxx xxxx	EUSART receive register
FAF	SPBRG	W	19	0001 1001	Serial port baud rate generator… 19,200bps
FB0	SPBRGH	-	xx	xxxx xxxx	Serial port baud rate generator high byte… Don't access
FB1	T3CON	W	00	0000 0000	Timer control… default
FB2	TMR3L	-	xx	xxxx xxxx	Timer3 register low byte… Don't access
FB3	TMR3H	-	xx	xxxx xxxx	Timer3 register high byte… Don't access
FB4	CMCON	W	07	0000 0111	Comparator control… Default
FB5	CVRCON	W	00	0000 0000	Comparator voltage reference… Default
FB6	ECCP1AS	W	00	0000 0000	ECCP auto-shutdown control… Default
FB7	PWM1CON	W	00	0000 0000	PWM dead-band delay… Default
FB8	BAUDCON	W	02	0000 0010	Baud rate control… Enable receive wake-up
FBA	CCP2CON	-	xx	xxxx xxxx	CCP2 control… Don't access
FBB	CCPR2L	-	xx	xxxx xxxx	Capture/compare/PWM register 2 low byte… Don't access
FBC	CCPR2H	-	xx	xxxx xxxx	Capture/compare/PWM register 2 high byte… Don't access
FBD	CCP1CON	W	0C	0000 1100	CCP1 control… PWM mode, LSBs of duty cycle (Set after T2CON)
FBE	CCPR1L	W	64	0110 0100	Capture/compare/PWM register 1 low byte… MSBs of duty cycle
FBF	CCPR1H	-	xx	xxxx xxxx	Capture/compare/PWM register 1 high byte… Don't access
FC0	ADCON2	W	21	0010 0001	A/D control 2… T_{ACQ}=8*T_{AD}, Clock=F_{OSC}/8
FC1	ADCON1	W	0E	0000 1110	A/D control 1… Port configuration (AN0 only)
FC2	ADCON0	W	0x	0000 00xx	A/D control 0… <1:0> are set in driver
FC3	ADRESL	-	xx	xxxx xxxx	A/D result low byte… Don't access
FC4	ADRESH	-	xx	xxxx xxxx	A/D result high byte… Don't access
FC5	SSPCON2	R/W	xx	0xxx xxxx	MSSP control 2… control Tx/Rx during communication
FC6	SSPCON1	R/W	28	0010 1000	MSSP control 1… Enabled as I^2C Master Mode
FC7	SSPSTAT	R/W	80	1000 0000	MSSP status (I^2C)… Standard speed (100kHz)
FC8	SSPADD	W	13	0001 0011	MSSP clock frequency… 100kHz
FC9	SSPBUF	R/W	xx	xxxx xxxx	MSSP Receive/Transmit buffer
FCA	T2CON	W	04	0000 0100	Timer2 control… Enabled, prescale=1:1 (Set after PR2, CCPR1L)
FCB	PR2	W	C8	1100 1000	Timer2 period… =200, 100[usec], 10[kHz]
FCC	TMR2	-	xx	xxxx xxxx	Timer2… Don't access
FCD	T1CON	W	00	0000 0000	Timer1 control… Default (disable)
FCE	TMR1L	-	xx	xxxx xxxx	Timer1 low byte… Don't access
FCF	TMR1H	-	xx	xxxx xxxx	Timer1 high byte… Don't access
FD0	RCON	W	DF	1101 1111	Reset control… Enable interrupt priority level
FD1	WDTCON	W	00	0000 0000	Watch dog timer control… Default (disable)
FD2	HLVDCON	W	05	0000 0101	High/low voltage detect control… Default (disable)
FD3	OSCCON	R/W	72	0111 0010	Oscillator control… Internal oscillator, 8MHz
FD5	T0CON	W	C3	1100 0011	Timer0 control… Enable, 8-bit, 1/16 prescale
FD6	TMR0L	W	81	1000 0011	Timer0 low byte… 1msec interval
FD7	TMR0H	-	xx	xxxx xxxx	Timer0 high byte… Don't access
FD8	STATUS	R	xx	xxxx xxxx	Status… Don't access
FD9	FSR2L	-	xx	xxxx xxxx	FSR2 (Data memory pointer) low byte… Don't access
FDA	FSR2H	-	xx	xxxx xxxx	FSR2 (Data memory pointer) high byte… Don't access

FDB	PLUSW2	-	xx	xxxx xxxx	Not physical register
FDC	PREINC2	-	xx	xxxx xxxx	Not physical register
FDD	POSTDEC2	-	xx	xxxx xxxx	Not physical register
FDE	POSTINC2	-	xx	xxxx xxxx	Not physical register
FDF	INDF2	-	xx	xxxx xxxx	Not physical register
FE0	BSR	-	xx	xxxx xxxx	Bank select… Don't access
FE1	FSR1L	-	xx	xxxx xxxx	FSR1 (Data memory pointer) low byte… Don't access
FE2	FSR1H	-	xx	xxxx xxxx	FSR1 (Data memory pointer) high byte… Don't access
FE3	PLUSW1	-	xx	xxxx xxxx	Not physical register
FE4	PREINC1	-	xx	xxxx xxxx	Not physical register
FE5	POSTDEC1	-	xx	xxxx xxxx	Not physical register
FE6	POSTINC1	-	xx	xxxx xxxx	Not physical register
FE7	INDF1	-	xx	xxxx xxxx	Not physical register
FE8	WREG	-	xx	xxxx xxxx	Working register… Don't access
FE9	FSR0L	-	xx	xxxx xxxx	FSR0 (Data memory pointer) low byte… Don't access
FEA	FSR0H	-	xx	xxxx xxxx	FSR0 (Data memory pointer) high byte… Don't access
FEB	PLUSW0	-	xx	xxxx xxxx	Not physical register
FEC	PREINC0	-	xx	xxxx xxxx	Not physical register
FED	POSTDEC0	-	xx	xxxx xxxx	Not physical register
FEE	POSTINC0	-	xx	xxxx xxxx	Not physical register
FEF	INDF0	-	xx	xxxx xxxx	Not physical register
FF0	INTCON3	W	C0	1100 0000	External interrupt control… disable(default)
FF1	INTCON2	W	F5	1111 0101	External and Timer0 interrupt control… Default
FF2	INTCON	W	E0	1110 0000	Interrupt control… enable interrupts, TMR0 int enable
FF3	PRODL	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF4	PRODH	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF5	TABLAT	-	xx	xxxx xxxx	Program memory table latch… Don't access
FF6	TBLPTRL	-	xx	xxxx xxxx	Program memory table pointer low byte… Don't access
FF7	TBLPTRH	-	xx	xxxx xxxx	Program memory table pointer high byte… Don't access
FF8	TBLPTRU	-	xx	xxxx xxxx	Program memory table pointer upper byte… Don't access
FF9	PCL	-	xx	xxxx xxxx	Program counter low byte (also defined as PCLAT)… Don't access
FFA	PCLATH	-	xx	xxxx xxxx	Program counter latch low byte… Don't access
FFB	PCLATU	-	xx	xxxx xxxx	Program counter latch upper byte… Don't access
FFC	STKPTR	-	xx	xxxx xxxx	Stack pointer… Don't access
FFD	TOSL	-	xx	xxxx xxxx	Top-of-stack low byte… Don't access
FFE	TOSH	-	xx	xxxx xxxx	Top-of-stack high byte… Don't access
FFF	TOSU	-	xx	xxxx xxxx	Top-of-stack upper byte… Don't access

Source files [v0.4]

Module	Source	Header	Description
MAIN	main.c V0.40	main.h V0.40	Control eVolume chip PGA2310 and selector relays
INIT	init.c V0.31	init.h V0.32	Enable Port A for I/F w/ PGA2310, ADC enabled
DIAG	diag.c V0.30	diag.h V0.30	Display gain data and actual gain
CNSL	cnsl.c V0.12	cnsl.h V0.11	Console service routines
INTR	intr.c V0.03	-	I2C communication and soft timers supported
DISP	disp.c V0.11	disp.h V0.11	Device drivers of display for other modules
VOLM	volm.c V0.12	volm.h V0.12	Read rotation angle of VR1, calculate gain data and actual gain, and set gain data to eVolume chip

Sequence

Sending data to PGA2310

1. De-assert SCLK: RA3=0

2. Assert nCS: RA2=0
3. Set Data<15>: RA4=0 or 1
4. Shift data to left by 1 bit
5. Assert SCLK: RA3=1
6. De-assert SCLK: RA3=0
7. Return to step-3 till all the bits are sent
8. De-assert nCS: RA2=1

Data Structure

Volm

Struct	Member	Bitwise	Description
volmCtrlData	BYTE GainData		Gain data to be set to PGA2310
	BYTE VoltageBuf	<15:6>:Voltage, <5:0>:0	Voltage data of VR1
	BYTE WritePnt		Pointer to voltage buffer

- BYTE: unsigned char, WORD: unsigned short

Ver.0.5

Control Volume (gain), Selector and display mode from Console.
Ver.0.50: Volume and Selector can be controlled by Console.
Ver.0.51: The settings saved in EEPROM and loaded at initialize.

Specifications

Commands

Name	Character	Description	Note
Vol+	+	Increase gain by 0.5dB	
Vol-	-	Decrease gain by 0.5dB	
Mute	0	Mute: Set gain data to 0	
Preset #1	1	Set gain to -40dB (normal mode) Start Test #1 (Diag mode)	
Preset #2	2	Set gain to -35dB (normal mode) Start Test #2 (Diag mode)	
Preset #3	3	Set gain to -30dB (normal mode) Start Test #3 (Diag mode)	
Preset #4	4	Set gain to -25dB (normal mode) Start Test #4 (Diag mode)	
Preset #5	5	Set gain to -20dB (normal mode) Start Test #5 (Diag mode)	
Preset #6	6	Set gain to -15dB (normal mode) Start Test #6 (Diag mode)	
Preset #7	7	Set gain to -10dB (normal mode) Start Test #7 (Diag mode)	
Preset #8	8	Set gain to -5dB (normal mode) Start Test #8 (Diag mode)	
Preset #9	9	Set gain to 0dB (normal mode) Start Test #9 (Diag mode)	
Select	s	Select next source	
	S	Select previous source	
Offset	o, O	Enter Balance Adjust mode to set offset of R-ch	
Decrease R-ch	l, L	Decrease offset of R-ch (acoustic image moves to left)	In Balance Adjust mode only
Increae R-ch	r, R	Increase offset of R-ch (acoustic image moves to right)	In Balance Adjust mode only
Resume	‘ ‘ (space)	Exit Balance or Diagnostics mode and enter normal mode	
Diag	t, T	Enter diagnostics mode	
Brighter	b, B	Increase intensity of display	

Darker	d, D	Decrease intensity of display	
No display	n, N	Disable Display: Display always off	
Permanent	p, P	Display always on	
Quick	Q	Turn off Display 3 seconds after user manipulation	
Analog	a, A	Keep Display off unless gain or select changed by command	

Display format
0.5dB: Turn of Seg-dp of Dig-0

Display mode

Display mode	Description	Note
Quick	Display turns on when user changes gain or select. Display turns off 3 seconds after the change.	Default *1
Permanent	Display is always on.	
Analog	Display turns on only when command changes gain or select. Display turns off 3 seconds after the change.	*1
Disable	Display is always off.	

*1: When gain or select is changed by command, Seg-dp of Dig-0~2 are turned on after numeric display turns off.

Configuration of MCU [v0.5]

Internal OSC used, WDT disabled and single-supply ICSP disabled.
Same as Ver.0.1.

SFR settings [v0.5]

Address	Name	R/W	Hex	Binary	Description
F80	PORTA	R	xx	1x0x xxx0	Status of Port A… Used for I/F w/ PGA2310 (BD4:U7)
F81	PORTB	R	0x	0000 0xxx	Status of Port B… Used for relays (BD4:RL1-6)
F82	PORTC	R	x0	00x0 0000	Status of Port C… RC5 is controlled by F/W. The other bits are always '0'
F84	PORTE	R	00	0000 0000	Status of Port E pins. Always 00h because Port E is disabled
F89	LATA	R/W	4E	0100 1110	Latch for Port A… Initial state of I/F w/ PGA2310
F8A	LATB	R/W	0x	0000 0xxx	Latch for Port B… Used for relays (BD4:RL1-6)
F8B	LATC	R/W	x0	00x0 0000	Latch for Port C… RC5 is used to blink LED
F92	TRISA	W	A1	1010 0001	Tristate control for Port A… RA1-4,6 are outputs
F93	TRISB	W	FB	1111 1000	Tristate control for Port B… RB0-2 are outputs
F94	TRISC	W	DB	1101 1011	Tristate control for Port C… RC2,5 are output
F9B	OSCTUNE	W	00	0000 0000	Default
F9D	PIE1	W	38	0011 1000	Rx/Tx int enable, MCCP (I2C) int enable
F9E	PIR1	R	00	0000 0000	Peripheral interrupt request flag
F9F	IPR1	W	CF	1100 1111	Peripheral interrupt priority… UART in low priority
FA0	PIE2	W	x0	000x 0000	Interrupt enable… <4>:EEPROM int enable
FA1	PIR2	R/W	x0	000x 0000	Peripheral interrupt request flag… <4>:EEPROM int flag
FA2	IPR2	W	EF	1110 1111	Peripheral interrupt priority…EEPROM in low priority
FA6	EECON1	R/W	0x	0000 xxxx	EEPROM control… Control EEPROM accesses
FA7	EECON2	W	xx	xxxx xxxx	EEPROM control… Write 55h and 0AAh before writing data
FA8	EEDATA	R/W	xx	xxxx xxxx	EEPROM data… Data written to or read from EEPROM
FA9	EEADR	W	xx	xxxx xxxx	EEPROM address… Written before read/write
FAB	RCSTA	W	90	1001 0000	Serial port receive status and control… Serial port enable
FAC	TXSTA	W	26	0010 0110	Serial port transmit status and control… Transmit disable Bit-5 (TXEN) is set after related registers are initialized)
FAD	TXREG	W	xx	xxxx xxxx	EUSART transmit register
FAE	RCREG	R	xx	xxxx xxxx	EUSART receive register
FAF	SPBRG	W	19	0001 1001	Serial port baud rate generator… 19,200bps
FB0	SPBRGH	-	xx	xxxx xxxx	Serial port baud rate generator high byte… Don't access

FB1	T3CON	W	00	0000 0000	Timer control… default
FB2	TMR3L	–	xx	xxxx xxxx	Timer3 register low byte… Don't access
FB3	TMR3H	–	xx	xxxx xxxx	Timer3 register high byte… Don't access
FB4	CMCON	W	07	0000 0111	Comparator control… Default
FB5	CVRCON	W	00	0000 0000	Comparator voltage reference… Default
FB6	ECCP1AS	W	00	0000 0000	ECCP auto-shutdown control… Default
FB7	PWM1CON	W	00	0000 0000	PWM dead-band delay… Default
FB8	BAUDCON	W	02	0000 0010	Baud rate control… Enable receive wake-up
FBA	CCP2CON	–	xx	xxxx xxxx	CCP2 control… Don't access
FBB	CCPR2L	–	xx	xxxx xxxx	Capture/compare/PWM register 2 low byte… Don't access
FBC	CCPR2H	–	xx	xxxx xxxx	Capture/compare/PWM register 2 high byte… Don't access
FBD	CCP1CON	W	0C	0000 1100	CCP1 control… PWM mode, LSBs of duty cycle (Set after T2CON)
FBE	CCPR1L	W	64	0110 0100	Capture/compare/PWM register 1 low byte… MSBs of duty cycle
FBF	CCPR1H	–	xx	xxxx xxxx	Capture/compare/PWM register 1 high byte… Don't access
FC0	ADCON2	W	21	0010 0001	A/D control 2… T_{ACQ}=8*T_{AD}, Clock=F_{OSC}/8
FC1	ADCON1	W	0E	0000 1110	A/D control 1… Port configuration (AN0 only)
FC2	ADCON0	W	0x	0000 00xx	A/D control 0… <1:0> are set in driver
FC3	ADRESL	–	xx	xxxx xxxx	A/D result low byte… Don't access
FC4	ADRESH	–	xx	xxxx xxxx	A/D result high byte… Don't access
FC5	SSPCON2	R/W	xx	0xxx xxxx	MSSP control 2… control Tx/Rx during communication
FC6	SSPCON1	R/W	28	0010 1000	MSSP control 1… Enabled as I^2C Master Mode
FC7	SSPSTAT	R/W	80	1000 0000	MSSP status (I^2C)… Standard speed (100kHz)
FC8	SSPADD	W	13	0001 0011	MSSP clock frequency… 100kHz
FC9	SSPBUF	R/W	xx	xxxx xxxx	MSSP Receive/Transmit buffer
FCA	T2CON	W	04	0000 0100	Timer2 control… Enabled, prescale=1:1 (Set after PR2, CCPR1L)
FCB	PR2	W	C8	1100 1000	Timer2 period… =200, 100[usec], 10[kHz]
FCC	TMR2	–	xx	xxxx xxxx	Timer2… Don't access
FCD	T1CON	W	00	0000 0000	Timer1 control… Default (disable)
FCE	TMR1L	–	xx	xxxx xxxx	Timer1 low byte… Don't access
FCF	TMR1H	–	xx	xxxx xxxx	Timer1 high byte… Don't access
FD0	RCON	W	DF	1101 1111	Reset control… Enable interrupt priority level
FD1	WDTCON	W	00	0000 0000	Watch dog timer control… Default (disable)
FD2	HLVDCON	W	05	0000 0101	High/low voltage detect control… Default (disable)
FD3	OSCCON	R/W	72	0111 0010	Oscillator control… Internal oscillator, 8MHz
FD5	T0CON	W	C3	1100 0011	Timer0 control… Enable, 8-bit, 1/16 prescale
FD6	TMR0L	W	81	1000 0011	Timer0 low byte… 1msec interval
FD7	TMR0H	–	xx	xxxx xxxx	Timer0 high byte… Don't access
FD8	STATUS	R	xx	xxxx xxxx	Status… Don't access
FD9	FSR2L	–	xx	xxxx xxxx	FSR2 (Data memory pointer) low byte… Don't access
FDA	FSR2H	–	xx	xxxx xxxx	FSR2 (Data memory pointer) high byte… Don't access
FDB	PLUSW2	–	xx	xxxx xxxx	Not physical register
FDC	PREINC2	–	xx	xxxx xxxx	Not physical register
FDD	POSTDEC2	–	xx	xxxx xxxx	Not physical register
FDE	POSTINC2	–	xx	xxxx xxxx	Not physical register
FDF	INDF2	–	xx	xxxx xxxx	Not physical register
FE0	BSR	–	xx	xxxx xxxx	Bank select… Don't access
FE1	FSR1L	–	xx	xxxx xxxx	FSR1 (Data memory pointer) low byte… Don't access
FE2	FSR1H	–	xx	xxxx xxxx	FSR1 (Data memory pointer) high byte… Don't access
FE3	PLUSW1	–	xx	xxxx xxxx	Not physical register
FE4	PREINC1	–	xx	xxxx xxxx	Not physical register
FE5	POSTDEC1	–	xx	xxxx xxxx	Not physical register
FE6	POSTINC1	–	xx	xxxx xxxx	Not physical register
FE7	INDF1	–	xx	xxxx xxxx	Not physical register
FE8	WREG	–	xx	xxxx xxxx	Working register… Don't access
FE9	FSR0L	–	xx	xxxx xxxx	FSR0 (Data memory pointer) low byte… Don't access
FEA	FSR0H	–	xx	xxxx xxxx	FSR0 (Data memory pointer) high byte… Don't access
FEB	PLUSW0	–	xx	xxxx xxxx	Not physical register

FEC	PREINC0	-	xx	xxxx xxxx	Not physical register
FED	POSTDEC0	-	xx	xxxx xxxx	Not physical register
FEE	POSTINC0	-	xx	xxxx xxxx	Not physical register
FEF	INDF0	-	xx	xxxx xxxx	Not physical register
FF0	INTCON3	W	C0	1100 0000	External interrupt control… disable(default)
FF1	INTCON2	W	F5	1111 0101	External and Timer0 interrupt control… Default
FF2	INTCON	W	E0	1110 0000	Interrupt control… enable interrupts, TMR0 int enable
FF3	PRODL	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF4	PRODH	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF5	TABLAT	-	xx	xxxx xxxx	Program memory table latch… Don't access
FF6	TBLPTRL	-	xx	xxxx xxxx	Program memory table pointer low byte… Don't access
FF7	TBLPTRH	-	xx	xxxx xxxx	Program memory table pointer high byte… Don't access
FF8	TBLPTRU	-	xx	xxxx xxxx	Program memory table pointer upper byte… Don't access
FF9	PCL	-	xx	xxxx xxxx	Program counter low byte (also defined as PCLAT)… Don't access
FFA	PCLATH	-	xx	xxxx xxxx	Program counter latch low byte… Don't access
FFB	PCLATU	-	xx	xxxx xxxx	Program counter latch upper byte… Don't access
FFC	STKPTR	-	xx	xxxx xxxx	Stack pointer… Don't access
FFD	TOSL	-	xx	xxxx xxxx	Top-of-stack low byte… Don't access
FFE	TOSH	-	xx	xxxx xxxx	Top-of-stack high byte… Don't access
FFF	TOSU	-	xx	xxxx xxxx	Top-of-stack upper byte… Don't access

Source files [v0.5]

Module	Source	Header	Description
MAIN	main.c v0.50 v0.51	main.h v0.50 v0.51	Command analysis Setting data saved to/ resumed from EEPROM
INIT	init.c v0.31 v0.40	init.h v0.32 v0.40	Enable Port A for I/F w/ PGA2310, ADC enabled EEPROM support
DIAG	diag.c v0.30	diag.h v0.30	Display gain data and actual gain
CNSL	cnsl.c v0.12	cnsl.h v0.11	Console service routines
INTR	intr.c v0.03 v0.04	-	I2C communication and soft timers supported EEPROM support
DISP	disp.c v0.21 v0.22	disp.h v0.21 v0.22	Device drivers of display for other modules Intensity setting routine added
VOLM	volm.c V0.20	volm.h V0.21	Read rotation angle of VR1, calculate gain data and actual gain, and set gain data to eVolume chip

Data Structure

Main

Struct	Member	Bitwise	Description
mainCtrlData	BYTE State		State
	BYTE PreviousState		Previous state
	BYTE Select		Selected source
	BYTE GainData		Value to be set to PGA2310, ch-L
	int OffsetR		GainData+Offset → ch-R *1
	BYTE Gain		Actual gain
	BYTE Fraction		Flag: fraction of gain (0.5dB) exists
	BYTE DisplayMode		Display mode *1
	BYTE Mismatched		Flag: Mismatch between display and knobs
	BYTE TimerOn		Flag: Timeout timer running
mainSoftTimer	WORD CntTickDiag		Tick for diagnostics
	WORD CntTickMain		Tick for main routine
	WORD CntTimeout		Timeout timer

- BYTE: unsigned char, WORD: unsigned short

*1: Saved in EEPROM. Resumed in start-up sequence

DISP

Struct	Member	Bitwise	Description
dispCtrlData	BYTE AddrRW		Slave address in I²C bus + R/W flag
	BYTE Command		Command to AS1115 (register address)
	BYTE Data[]		Register data to/from AS1115
	BYTE Status		Status of DISP module
	BYTE State		State of I²C Bus
	BYTE Request		Request to I²C Bus
	BYTE DataCnt		Data counter for multiple data transfer via I²C Bus
	BYTE NumBytes		The number of bytes to be transferred via I²C Bus
	BYTE Inten		Intensity of Display

INIT

Struct	Member	Bitwise	Description
initEEPROM	BYTE OffsetL		Low byte of Offset gain (OffsetR in mainCtrlData)
	BYTE OffsetH		High byte of Offset gain (OffsetR in mainCtrlData)
	BYTE DispMode		Display mode (DisplayMode in mainCtrlData)
	BYTE Inten		Intensity of Display (Inten in dispCtrlData)

State Machine of Display

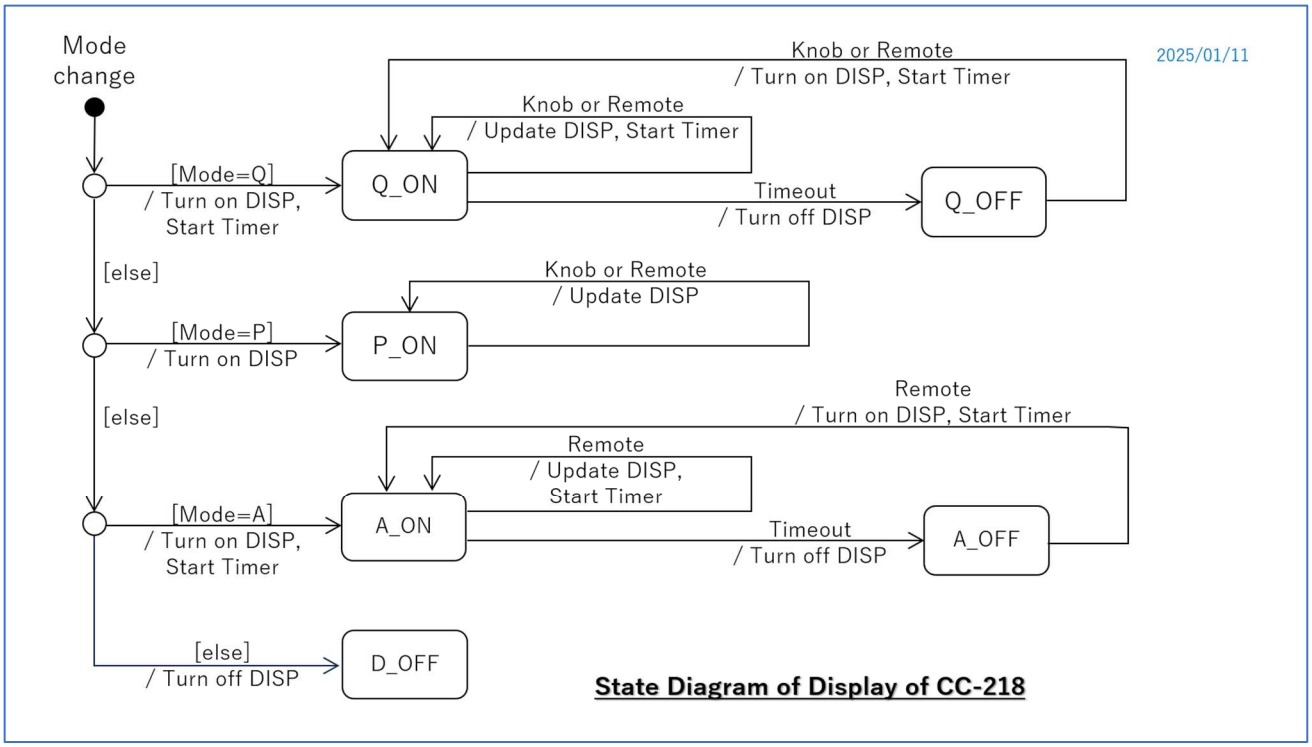
Fraction sign
When actual gain includes fraction (0.5dB), Dig-0:Seg-dp turns on.

State table

State	Previous State	Entry	Do	Exit	Note
Q_ON	(any)	Turn on DISP Start Timer	DISP on	(none)	Quick mode w/ Display on
Q_OFF	Q_ON	Turn off DISP	DISP off w/ fraction sign	(none)	Quick mode w/ Display off
P_ON	(any)	Turn on DISP	DISP on	(none)	Permanent mode
A_ON	(any)	Turn on DISP Start Timer	DISP on	(none)	Analog mode w/ Display on
A_OFF	A_ON	Turn of DISP	DISP off w/ fraction sign	(none)	Analog mode w/ Display off
D_OFF	(any)	Turn off DISP	DISP off	(none)	Disable mode

DISP: Numeric display and Indicator
Timer: Timeout timer (Soft timer)

State chart



EEPROM Access Sequences

Read sequence

(1) Address → EEADR
(2) EEPGD=0, CFGS=0 → EECON1
(3) RD=1 → EECON1
(4) Read EEDATA

Write sequence

(1) Address → EEADR
(2) Data → EEDATA
(3) EEPGD=0, CFGS=0, WREN=1 → EECON1
(4) Disable interrupt
(5) 55h → EECON2
(6) 0AAh → EECON2
(7) WR=1 → EECON1
(8) Enable interrupt
(9) Interrupt occurs ➔ WREN=0 → EECON1

Ver.0.6

Commands that are common with those issued by Console are received from IR Remote.
Ver.0.60: Receive codes from IR Remote, and display them on Console.
Ver.0.61: Convert codes received from IR Remote to commands, and execute them.
Ver.0.62: Support muting feature with fade-in/fade-out.

Specifications

IR Remote spec

No	Name	Button	Description	Corresponding Console command
10	Vol+	+ (大)	Increase gain by 0.5dB (normal mode) Increase offset by 0.5dB (Balance Adjust mode)	+
11	Vol-	- (小)	Decrease gain by 0.5dB (normal mode) Decrease offset by 0.5dB (Balance Adjust mode)	-
0	Preset #0	0 / 10	Set gain data to 0 (gain=-∞dB)	0
1	Preset #1	1	Set gain to -40dB (normal mode)	1
2	Preset #2	2	Set gain to -35dB (normal mode)	2
3	Preset #3	3	Set gain to -30dB (normal mode)	3
4	Preset #4	4	Set gain to -25dB (normal mode)	4
5	Preset #5	5	Set gain to -20dB (normal mode)	5
6	Preset #6	6	Set gain to -15dB (normal mode)	6
7	Preset #7	7	Set gain to -10dB (normal mode)	7
8	Preset #8	8	Set gain to -5dB (normal mode)	8
9	Preset #9	9	Set gain to 0dB (normal mode)	9
12	Offset	AUDIO (音声切換)	Enter/exit Balance Adjust mode	o, O
13	Sel+	CH+ (+)	Next select pattern *1	s
14	Sel-	CH- (-)	Previous select pattern *1	S
15	Intensity	SELECT (入力切換)	Increase intensity of display *2	b, B
16	Display mode	Display (画面表示)	Change Display mode: Quick → Permanent → Analog → Disabled → Quick → …	(no equivalent command)
17	Mute	MUTE(消音)	Set gain data to 0 when gain is not 0 Set gain data to the previous one when gain is 0	(no equivalent command)

*1: PHONO, DAC, AUX, DAC+AUX, PHONO+AUX, PHONO+DAC, PHONO+DAC+AUX, none
*2: LEVEL1, LEVEL2, LEVEL3, …, LEVEL7 (LEVEL1 is darkest, LEVEL7 is brightest)

Configuration of MCU [v0.6]

Internal OSC used, WDT disabled and single-supply ICSP disabled.
Same as Ver.0.1.

SFR settings [v0.6]

Address	Name	R/W	Hex	Binary	Description
F80	PORTA	R	xx	1x0x xxx0	Status of Port A… Used for I/F w/ PGA2310 (BD4:U7)
F81	PORTB	R	0x	0000 0xxx	Status of Port B… Used for relays (BD4:RL1-6)
F82	PORTC	R	x0	00x0 0000	Status of Port C… RC5 is controlled by F/W. The other bits are always '0'
F84	PORTE	R	00	0000 0000	Status of Port E pins. Always 00h because Port E is disabled
F89	LATA	R/W	4E	0100 1110	Latch for Port A… Initial state of I/F w/ PGA2310
F8A	LATB	R/W	1x	0001 0xxx	Latch for Port B… Used for relays (BD4:RL1-6), RB4=1 for int
F8B	LATC	R/W	x0	00x0 0000	Latch for Port C… RC5 is used to blink LED
F92	TRISA	W	A1	1010 0001	Tristate control for Port A… RA1-4,6 are outputs
F93	TRISB	W	FB	1111 1000	Tristate control for Port B… RB0-2 are outputs
F94	TRISC	W	DB	1101 1011	Tristate control for Port C… RC2,5 are output
F9B	OSCTUNE	W	00	0000 0000	Default
F9D	PIE1	W	39	0011 1001	Rx/Tx int enable, MCCP (I2C) int enable
F9E	PIR1	R/W	00	00xx 000x	Peripheral interrupt request flag
F9F	IPR1	W	CE	1100 1110	Peripheral interrupt priority… UART, TIMER1 in low priority
FA0	PIE2	W	x0	000x 0000	Interrupt enable… <4>:EEPROM int enable
FA1	PIR2	R/W	x0	000x 0000	Peripheral interrupt request flag… <4>:EEPROM int flag
FA2	IPR2	W	EF	1110 1111	Peripheral interrupt priority…EEPROM in low priority
FA6	EECON1	R/W	0x	0000 xxxx	EEPROM control… Control EEPROM accesses
FA7	EECON2	W	xx	xxxx xxxx	EEPROM control… Write 55h and 0AAh before writing data
FA8	EEDATA	R/W	xx	xxxx xxxx	EEPROM data… Data written to or read from EEPROM
FA9	EEADR	W	xx	xxxx xxxx	EEPROM address… Written before read/write

FAB	RCSTA	W	90	1001 0000	Serial port receive status and control… Serial port enable
FAC	TXSTA	W	26	0010 0110	Serial port transmit status and control… Transmit disable Bit-5 (TXEN) is set after related registers are initialized)
FAD	TXREG	W	xx	xxxx xxxx	EUSART transmit register
FAE	RCREG	R	xx	xxxx xxxx	EUSART receive register
FAF	SPBRG	W	19	0001 1001	Serial port baud rate generator… 19,200bps
FB0	SPBRGH	–	xx	xxxx xxxx	Serial port baud rate generator high byte… Don't access
FB1	T3CON	W	00	0000 0000	Timer control… default
FB2	TMR3L	–	xx	xxxx xxxx	Timer3 register low byte… Don't access
FB3	TMR3H	–	xx	xxxx xxxx	Timer3 register high byte… Don't access
FB4	CMCON	W	07	0000 0111	Comparator control… Default
FB5	CVRCON	W	00	0000 0000	Comparator voltage reference… Default
FB6	ECCP1AS	W	00	0000 0000	ECCP auto-shutdown control… Default
FB7	PWM1CON	W	00	0000 0000	PWM dead-band delay… Default
FB8	BAUDCON	W	02	0000 0010	Baud rate control… Enable receive wake-up
FBA	CCP2CON	–	xx	xxxx xxxx	CCP2 control… Don't access
FBB	CCPR2L	–	xx	xxxx xxxx	Capture/compare/PWM register 2 low byte… Don't access
FBC	CCPR2H	–	xx	xxxx xxxx	Capture/compare/PWM register 2 high byte… Don't access
FBD	CCP1CON	W	0C	0000 1100	CCP1 control… PWM mode, LSBs of duty cycle (Set after T2CON)
FBE	CCPR1L	W	64	0110 0100	Capture/compare/PWM register 1 low byte… MSBs of duty cycle
FBF	CCPR1H	–	xx	xxxx xxxx	Capture/compare/PWM register 1 high byte… Don't access
FC0	ADCON2	W	21	0010 0001	A/D control 2… T_{ACQ}=8*T_{AD}, Clock=F_{OSC}/8
FC1	ADCON1	W	0E	0000 1110	A/D control 1… Port configuration (AN0 only)
FC2	ADCON0	W	0x	0000 00xx	A/D control 0… <1:0> are set in driver
FC3	ADRESL	–	xx	xxxx xxxx	A/D result low byte… Don't access
FC4	ADRESH	–	xx	xxxx xxxx	A/D result high byte… Don't access
FC5	SSPCON2	R/W	xx	0xxx xxxx	MSSP control 2… control Tx/Rx during communication
FC6	SSPCON1	R/W	28	0010 1000	MSSP control 1… Enabled as I^2C Master Mode
FC7	SSPSTAT	R/W	80	1000 0000	MSSP status (I^2C)… Standard speed (100kHz)
FC8	SSPADD	W	13	0001 0011	MSSP clock frequency… 100kHz
FC9	SSPBUF	R/W	xx	xxxx xxxx	MSSP Receive/Transmit buffer
FCA	T2CON	W	04	0000 0100	Timer2 control… Enabled, prescale=1:1 (Set after PR2, CCPR1L)
FCB	PR2	W	C8	1100 1000	Timer2 period… =200, 100[usec], 10[kHz]
FCC	TMR2	–	xx	xxxx xxxx	Timer2… Don't access
FCD	T1CON	R/W	9x	1001 000x	Timer1 control… Used as 16-bit timer, prescale 1:2
FCE	TMR1L	R/W	xx	xxxx xxxx	Timer1 low byte
FCF	TMR1H	R/W	xx	xxxx xxxx	Timer1 high byte
FD0	RCON	W	DF	1101 1111	Reset control… Enable interrupt priority level
FD1	WDTCON	W	00	0000 0000	Watch dog timer control… Default (disable)
FD2	HLVDCON	W	05	0000 0101	High/low voltage detect control… Default (disable)
FD3	OSCCON	R/W	72	0111 0010	Oscillator control… Internal oscillator, 8MHz
FD5	T0CON	W	C3	1100 0011	Timer0 control… Enable, 8-bit, 1/16 prescale
FD6	TMR0L	W	81	1000 0011	Timer0 low byte… 1msec interval
FD7	TMR0H	–	xx	xxxx xxxx	Timer0 high byte… Don't access
FD8	STATUS	R	xx	xxxx xxxx	Status… Don't access
FD9	FSR2L	–	xx	xxxx xxxx	FSR2 (Data memory pointer) low byte… Don't access
FDA	FSR2H	–	xx	xxxx xxxx	FSR2 (Data memory pointer) high byte… Don't access
FDB	PLUSW2	–	xx	xxxx xxxx	Not physical register
FDC	PREINC2	–	xx	xxxx xxxx	Not physical register
FDD	POSTDEC2	–	xx	xxxx xxxx	Not physical register
FDE	POSTINC2	–	xx	xxxx xxxx	Not physical register
FDF	INDF2	–	xx	xxxx xxxx	Not physical register
FE0	BSR	–	xx	xxxx xxxx	Bank select… Don't access
FE1	FSR1L	–	xx	xxxx xxxx	FSR1 (Data memory pointer) low byte… Don't access
FE2	FSR1H	–	xx	xxxx xxxx	FSR1 (Data memory pointer) high byte… Don't access
FE3	PLUSW1	–	xx	xxxx xxxx	Not physical register
FE4	PREINC1	–	xx	xxxx xxxx	Not physical register

FE5	POSTDEC1	-	xx	xxxx xxxx	Not physical register
FE6	POSTINC1	-	xx	xxxx xxxx	Not physical register
FE7	INDF1	-	xx	xxxx xxxx	Not physical register
FE8	WREG	-	xx	xxxx xxxx	Working register… Don't access
FE9	FSR0L	-	xx	xxxx xxxx	FSR0 (Data memory pointer) low byte… Don't access
FEA	FSR0H	-	xx	xxxx xxxx	FSR0 (Data memory pointer) high byte… Don't access
FEB	PLUSW0	-	xx	xxxx xxxx	Not physical register
FEC	PREINC0	-	xx	xxxx xxxx	Not physical register
FED	POSTDEC0	-	xx	xxxx xxxx	Not physical register
FEE	POSTINC0	-	xx	xxxx xxxx	Not physical register
FEF	INDF0	-	xx	xxxx xxxx	Not physical register
FF0	INTCON3	W	C0	1100 0000	External interrupt control… disable(default)
FF1	INTCON2	W	F5	1111 0101	External and Timer0 interrupt control… Default
FF2	INTCON	R/W	Ex	1110 x00x	Interrupt control… enable interrupts, TMR0 int enabled, RB int enabled
FF3	PRODL	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF4	PRODH	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF5	TABLAT	-	xx	xxxx xxxx	Program memory table latch… Don't access
FF6	TBLPTRL	-	xx	xxxx xxxx	Program memory table pointer low byte… Don't access
FF7	TBLPTRH	-	xx	xxxx xxxx	Program memory table pointer high byte… Don't access
FF8	TBLPTRU	-	xx	xxxx xxxx	Program memory table pointer upper byte… Don't access
FF9	PCL	-	xx	xxxx xxxx	Program counter low byte (also defined as PCLAT)… Don't access
FFA	PCLATH	-	xx	xxxx xxxx	Program counter latch low byte… Don't access
FFB	PCLATU	-	xx	xxxx xxxx	Program counter latch upper byte… Don't access
FFC	STKPTR	-	xx	xxxx xxxx	Stack pointer… Don't access
FFD	TOSL	-	xx	xxxx xxxx	Top-of-stack low byte… Don't access
FFE	TOSH	-	xx	xxxx xxxx	Top-of-stack high byte… Don't access
FFF	TOSU	-	xx	xxxx xxxx	Top-of-stack upper byte… Don't access

Source files [v0.6]

Module	Source	Header	Description
MAIN	main.c v0.60 v0.61 v0.62	main.h v0.60 v0.61 v0.62	Get codes from IR Remote Convert codes into commands and execute them Support muting w/ fade-in/fade-out
INIT	init.c v0.50	init.h v0.52	Initialize REMT module
DIAG	diag.c v0.30 v0.31	diag.h v0.30	Display gain data and actual gain Startup display simplified
CNSL	cnsl.c v0.12	cnsl.h v0.11	Console service routines
INTR	intr.c v0.05	-	Handle PORTB and Timer1 interrupts
DISP	disp.c v0.23	disp.h v0.23	Device drivers of display for other modules
VOLM	volm.c v0.20	volm.h v0.21	Read rotation angle of VR1, calculate gain data and actual gain, and set gain data to eVolume chip
REMT	remt.c v0.00 v0.10	remt.h v0.00 v0.10	Receive codes from IR Remote Convert received code into commands, and execute them

Data Structure [v0.6]

REMT

Struct	Member	Bitwise	Description
remtCtrlData	BYTE State		State of IR remote state machine
	BYTE Command		Last command received from IR Remote
remtIrCode	BYTE NumCodes		Number of codes received
	WORD Code[]		Codes received from IR Remote

	BYTE Valid		Valid flag: Code packet successfully received

- BYTE: unsigned char, WORD: unsigned short

Method to Receive Signal from IR Receiver

Let interrupt occur when the state of nIR_IN (RB4) changes.

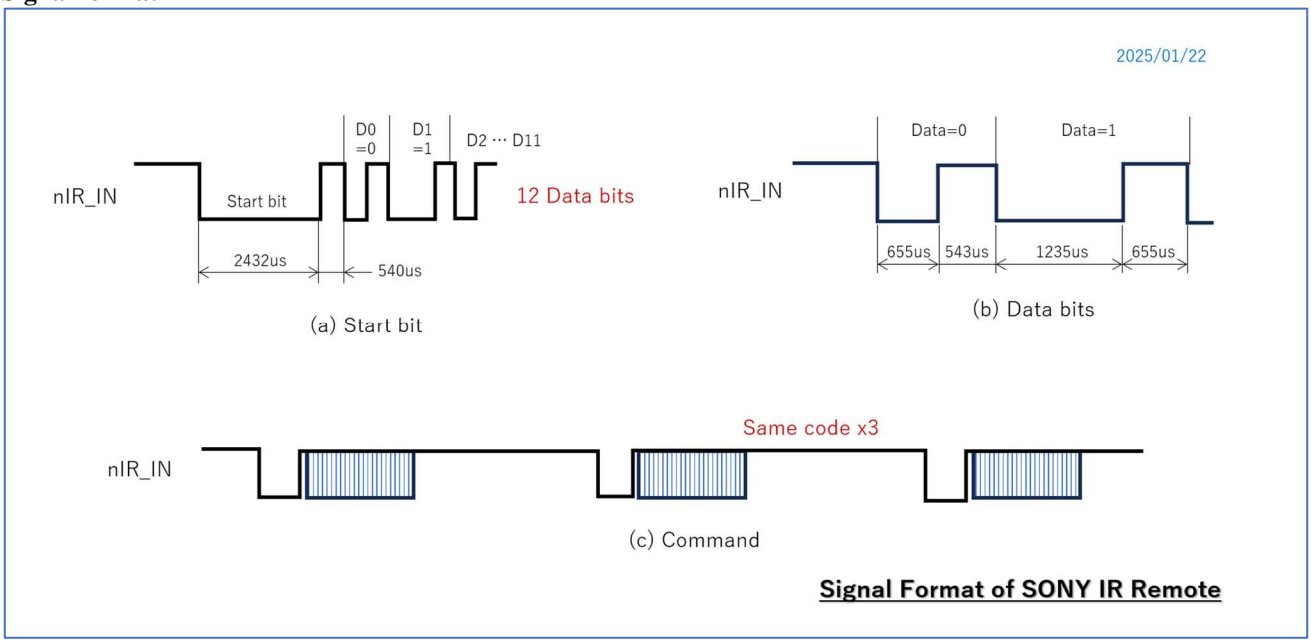
PORTB
LATB<4> = 1
This means interrupt occurs when RB4 = 0, because it mismatches the value of LATB.
LATB<4> = 0
This means interrupt occurs when RB4 = 1, because it mismatches the value of LATB.

Interrupt control
INTCON2<0> = 1 (PORTB interrupt in high priority)
INTCON<3>(RBIE) = 1 when monitoring RB4 is ready

Sequence to measure pulse width
(1) LATB<4> = 1
(2) INTCON<3>(RBIE) = 1 (enable interrupt)
(3) Interrupt → Start Timer1, Clear INTCON<0>(EBIF), Read PORTB (interrupt request is terminated)
(4) LATB<4> = 0
(5) Interrupt → Stop Timer1, Clear INTCON<0>(EBIF), Read PORTB (interrupt request is terminated)
(6) Read Timer1 (TMR1L, TMR1H) → Get the pulse width

Timer1 clock = 1MHz → Timer1 counts up every 1usec
Timer1 overflows after 65,536us elapses → this means the signal from IR Remote is interfered by some reason
→ Reset state machine to Idle state.

Signal format



Pulse widths (unit: usec)

Symbol	Shortest	Nominal	Longest	Definition
START_A	2,000	2,400	-	Start bit active time
INACTIVE	-	600	1,000	Inactive time
DATA_A_0		650	1,000	Data active time for '0'
DATA_A_1	1,000	1,235	-	Data active time for '1'

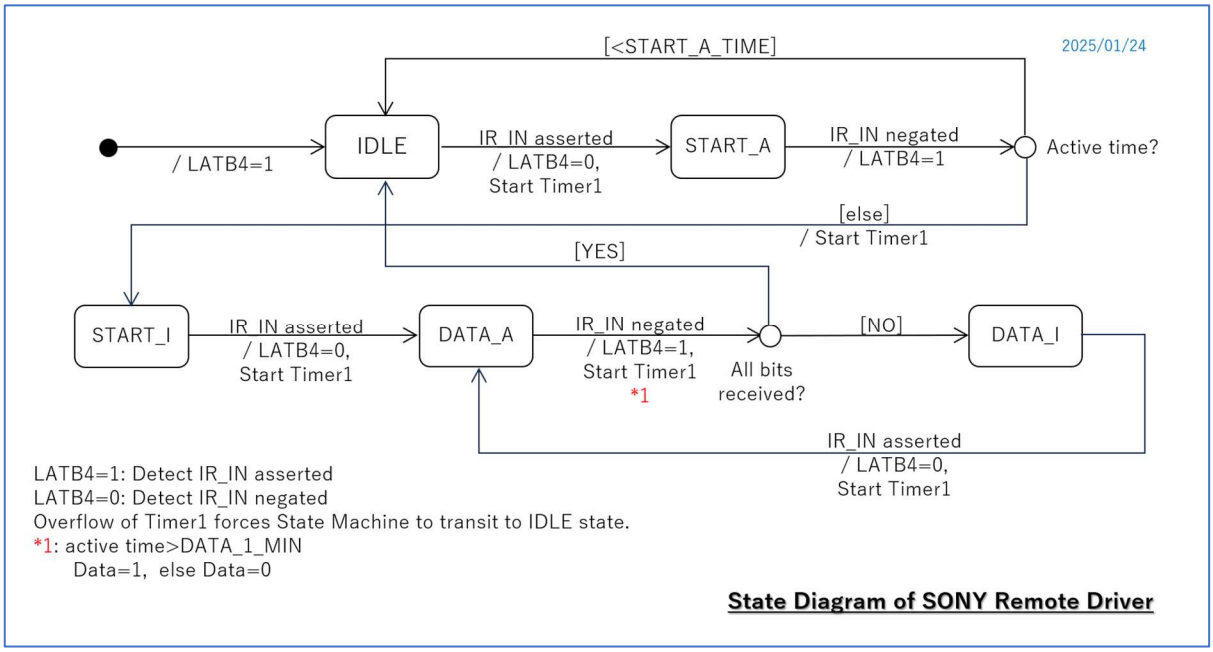
State Machine of IR Interface

State table

State	Previous State	Entry	Do	Exit	Note
IDLE	(intialize) START_A DATA_I (timeout)	LATB4=1	(none)	(none)	IR_IN inactive period
START_A	IDLE	LATB4=0 Start Timer1	(none)	LATB4=1	Start bit active period
START_I	START_A	Start Timer1	(none)		Start bit inactive period
DATA_A	START_I DATA_I	LATB4=0 Start Timer1	(none)	(none)	Data bit active period
DATA_I	DATA_A	LATB4=1 Start Timer1	(none)	LATB4=0 Start Timer1	Data bit inactive period to DATA_A
				LATB4=1	Data bit inactive period to IDLE

REPEAT: Repeat code flag
Timer: Timer1 (counted up at every 1usec)

State chart



Ver.0.7

CC-218 FW plays master role, when slave device is connected to CC-218.
Ver.0.70: Send commands to slave device while maintaining the gain at +/-0dB.

Specifications

Master mode request added to commands.
When CC-218 receives this command, it will get into Master mode where gain keeps +/-0dB all the time and send gain data to slave whenever volume change is requested by user.
Once CC-218 enters Master mode, the mode is maintained till shutdown.
The default mode of CC-218 is Stand Alone mode.

Console commands

Name	Character	Description	Note
Vol+	+	Increase gain by 0.5dB	
Vol-	-	Decrease gain by 0.5dB	
Mute	0	Transit to Mute mode: Fade out to gain data 0 Transit from Mute mode: Fade in from gain data 0 to previous gain	
Preset #1	1	Set gain to -40dB (normal mode) Start Test #1 (Diag mode)	
Preset #2	2	Set gain to -35dB (normal mode) Start Test #2 (Diag mode)	
Preset #3	3	Set gain to -30dB (normal mode) Start Test #3 (Diag mode)	
Preset #4	4	Set gain to -25dB (normal mode) Start Test #4 (Diag mode)	
Preset #5	5	Set gain to -20dB (normal mode) Start Test #5 (Diag mode)	
Preset #6	6	Set gain to -15dB (normal mode) Start Test #6 (Diag mode)	
Preset #7	7	Set gain to -10dB (normal mode) Start Test #7 (Diag mode)	
Preset #8	8	Set gain to -5dB (normal mode) Start Test #8 (Diag mode)	
Preset #9	9	Set gain to 0dB (normal mode) Start Test #9 (Diag mode)	
Select	s	Select next source	
	S	Select previous source	
Offset	o, O	Enter Balance Adjust mode to set offset of R-ch	
Decrease R-ch	l, L	Decrease offset of R-ch (acoustic image moves to left)	In Balance Adjust mode only
Increae R-ch	r, R	Increase offset of R-ch (acoustic image moves to right)	In Balance Adjust mode only
Resume	‘ ‘ (space)	Exit Balance or Diagnostics mode and enter normal mode	
Diag	t, T	Enter diagnostics mode	
Brighter	b, B	Increase intensity of display	
Darker	d, D	Decrease intensity of display	
No display	n, N	Disable Display: Display always off	
Permanent	p, P	Display always on	
Quick	Q	Turn off Display 3 seconds after user manipulation	
Analog	a, A	Keep Display off unless gain or select changed by command	
Master	m, M	Master mode request… Get into Master mode	

Master-to-slave commands

1. Slave mode request
   Function: Request the slave device to enter Slave mode.
   Format: S or s
2. Gain data
   Function: Send gain data.
   Format: Lm Rn
   where m is the gain data of the left channel, and n is that of the right, both ranging 0~255.
   Example: L141 R143 → Gain data of the left channel is 141, the right channel is 143.
   It can be “l141 r143” (case insensitive).

Configuration of MCU [v7.0]

SFR values are the same as v0.6

Source files [v0.7]

Module	Source	Header	Description
MAIN	main.c v0.70	main.h v0.70	Implement Master mode
INIT	init.c v0.50	init.h v0.52	Initialize REMT module
DIAG	diag.c v0.31	diag.h v0.30	Display gain data and actual gain
CNSL	cnsl.c v0.12	cnsl.h v0.11	Console service routines
INTR	intr.c v0.05	-	Handle PORTB and Timer1 interrupts
DISP	disp.c v0.23	disp.h v0.23	Device drivers of display for other modules
VOLM	volm.c v0.30	volm.h v0.30	Read rotation angle of VR1, calculate gain data and actual gain, and set gain data to eVolume chip
REMT	remt.c v0.10	remt.h v0.10	Receive codes from IR Remote

Ver.1.0

Ver.1.0 is the final version of CC-218 FW, the firmware which controls CC-218 Stereo Control Center.
Ver1.0 is based on Ver.070. Watch dog timer (WDT) feature has been added to improve reliability.
WDT stops CPU runaway, in case.

Structure

Ordinary stand-alone structure.
This firmware acts like multitasking system (quasi-multitasking system). Each task executes (an) action(s), and exits soon, so that the main loop is executed within 50msec.

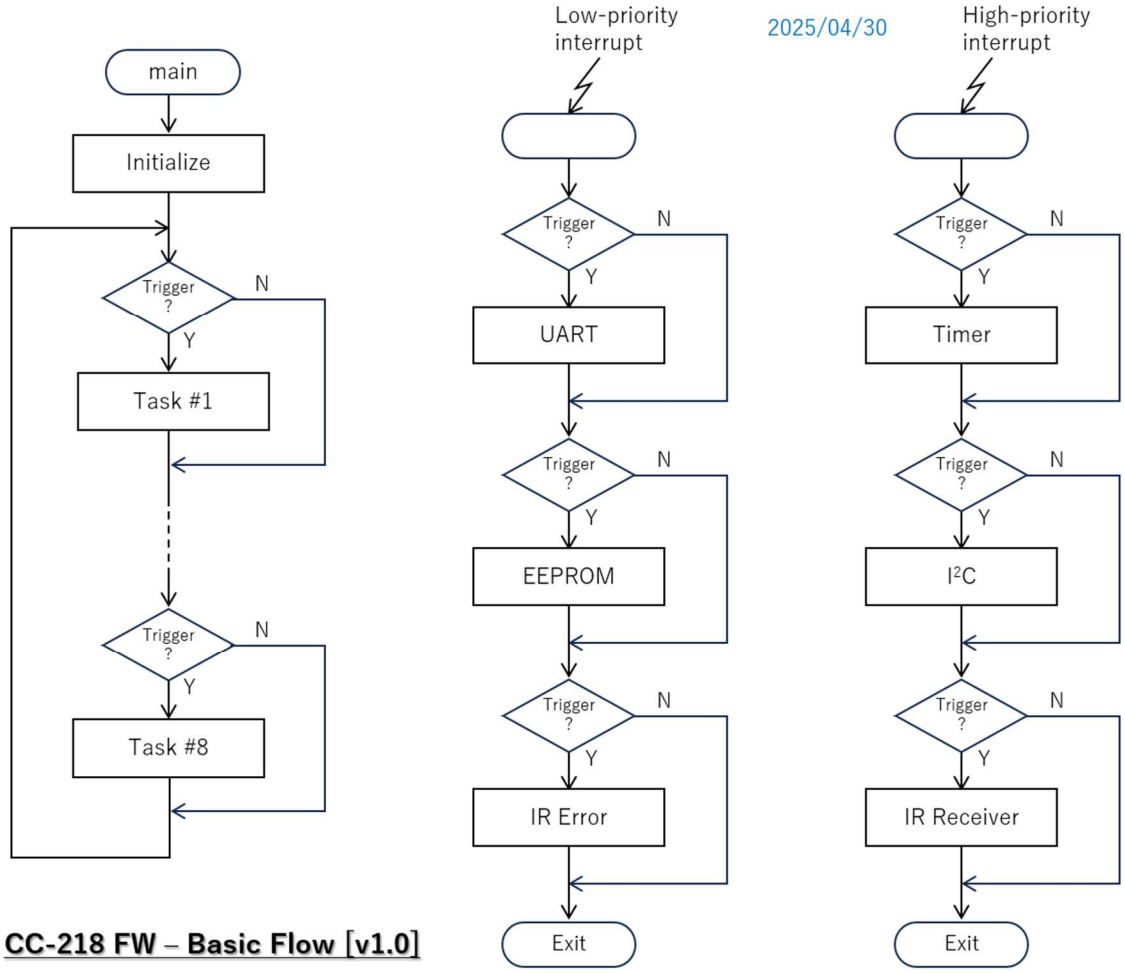
Tasks

CC-218 FW v1.0 consists of 8 tasks.

Task #	Task name	Trigger	Action
1	Execute Console Command	Receive command from Console	Parse and execute the command
2	Execute Remote Command	Receive command from Remote	Parse and execute the command
3	Execute Test Program	Firmware in Diagnostics mode	Execute test program Exit Diagnostics mode if test is over
4	Execute Test Program at Tick	Firmware in Diagnostics mode, and Diag Tick takes place	Execute test program Exit Diagnostics mode if test is over
5	Gain Control	Main Tick takes place, and VR1 is turned	Get gain by calculating rotation angle Set gain to eVolume chip Display the gain
6	Selector Control	Main Tick takes place, and SW2 is turned	Read SW2 Drive selector relay to select the source Indicate the source selected
7	Muting	Firmware in Muting mode, and Main Tick takes place	Decrease gain, or increase gain Display the gain
8	Display Timeout	3 seconds after Display changed last	Turn off display in certain Display modes

Flow

The following figure shows the overall flow of CC-218 FW.



CC-218 FW – Basic Flow [v1.0]

Interrupts

Low-priority interrupts

ISR	Source	Cause	Action
UART	UART (EUSART)	Transmit Register empty	Move transmit data from FIFO to Transmit Register if FIFO is not empty
		Receive Register full	Move receive data from Receive Register to FIFO
EEPROM	EEPROM	Write operation is complete	Check if error occurred
IR Error	Timer1	Timer1 overflow (Infra-red signal disrupted)	Reset state machine of IR remote

High-priority interrupts

ISR	Source	Cause	Action
Timer	Timer0	Timer0 overflow	Count down soft timers
I^2C	MSSP	Transmit/receive complete	Trigger state machine of I^2C driver
IR Receiver	PORTB	Transition of infra-red signal (nIR_IN)	Trigger state machine of IR remote

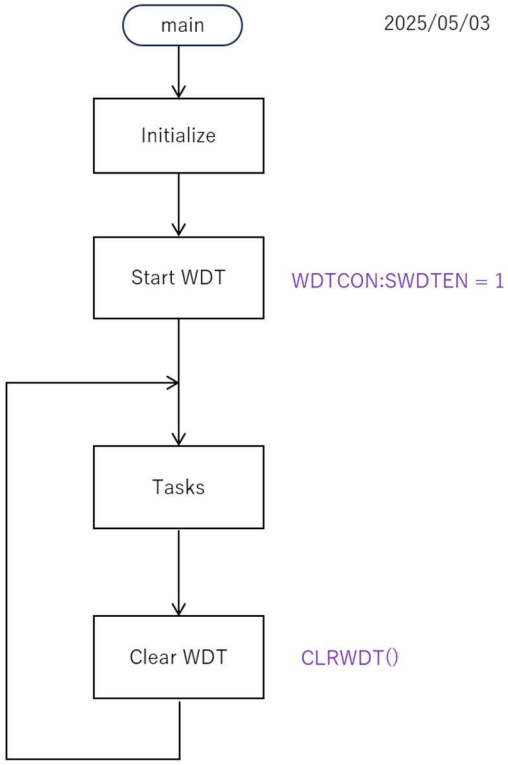
Modules

Module	Source	Header	Description
MAIN	main.c v1.00	main.h v1.00	Main module
INIT	init.c v0.50	init.h v0.52	Initialize system and peripherals
DIAG	diag.c v0.31	diag.h v0.30	Test programs
CNSL	cnsl.c v0.12	cnsl.h v0.11	Console service routines

INTR	intr.c v0.05	-	Interrupt service routines (ISRs)
DISP	disp.c v0.23	disp.h v0.23	Device driver of Display
VOLM	volm.c v0.30	volm.h v0.30	Read rotation angle of VR1, calculate gain data and actual gain, and set gain data to eVolume chip
REMT	remt.c v0.10	remt.h v0.10	Receive commands from IR Remote

Reliability

To improve reliability, watch dog timer is used.
To clear WDT, CLRWDT() macro is used, which the compiler XC8 offers for clearing WDT.
Flowchart of WDT:



CC-218 FW – Flowchart of WDT

Settings of MCU chip

Configuration registers

The final settings of the configuration registers of PIC18F2520 are shown in the following table.

Name	Value	Field	Option	Category	Setting
CONFIG1H	8	-	-	-	-
	8	OSC	INTIO67	Oscillator Selection bits	Internal oscillator block port function on RA6 and RA7
	0	FCMEN	OFF	Fail-Safe Clock Monitor Enable bit	Fail-Safe Clock Monitor disabled
	0	IESO	OFF	Internal/External Oscillator Switchover bit	Oscillator Switchover mode disabled
CONFIG2L	1F	-	-	-	-
	1	PWRT	OFF	Power-up Timer Enable bit	PWRT disabled
	3	BOREN	SBORDIS	Brown-out Reset Enable bits	Brown-out Reset enabled in hardware only (SBOREN is disabled)
	3	BORV	3	Brown Out Reset Voltage bits	Minimum setting
CONFIG2H	10	-	-	-	-
	0	WDT	OFF	Watchdog Timer Enable bit	WDT disabled (control is placed on the SWDTEN bit)
	8	WDTPS	256	Watchdog Timer Postscale Select bits	1:256… WDT provokes reset 1.024sec after the last write
CONFIG3H	1	-	-	-	-
	1	CCP2MX	PORTC	CCP2 MUX bit	CCP2 input/output is multiplexed with RC1
	0	PBADEN	OFF	PORTB A/D Enable bit	PORTB<4:0> pins are configured as digital I/O on Reset
	0	LPT1OSC	OFF	Low-Power Timer1 Oscillator Enable bit	Timer1 configured for higher power operation
	0	MCLRE	OFF	MCLR Pin Enable bit	RE3 input pin enabled; MCLR disabled
CONFIG4L	81	-	-	-	-
	1	STVREN	ON	Stack Full/Underflow Reset Enable bit	Stack full/underflow will cause Reset
	0	LVP	OFF	Single-Supply ICSP Enable bit	Single-Supply ICSP disabled
	0	XINST	OFF	Extended Instruction Set Enable bit	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
CONFIG5L	0F	-	-	-	-
	1	CP0	OFF	Code Protection bit	Block 0 (000800-001FFFh) not code-protected
	1	CP1	OFF	Code Protection bit	Block 1 (002000-003FFFh) not code-protected
	1	CP2	OFF	Code Protection bit	Block 2 (004000-005FFFh) not code-protected
	1	CP3	OFF	Code Protection bit	Block 3 (006000-007FFFh) not code-protected
CONFIG5H	C0	-	-	-	-
	1	CPB	OFF	Boot Block Code Protection bit	Boot block (000000-0007FFh) not code-protected
	1	CPD	OFF	Data EEPROM Code Protection bit	Data EEPROM not code-protected
CONFIG6L	0F	-	-	-	-
	1	WRT0	OFF	Write Protection bit	Block 0 (000800-001FFFh) not write-protected

	1	WRT1	OFF	Write Protection bit	Block 1 (002000-003FFFh) not write-protected
	1	WRT2	OFF	Write Protection bit	Block 2 (004000-005FFFh) not write-protected
	1	WRT3	OFF	Write Protection bit	Block 3 (006000-007FFFh) not write-protected
CONFIG6H	E0	-	-	-	-
	1	WRTC	OFF	Configuration Register Write Protection bit	Configuration registers (300000-3000FFh) not write-protected
	1	WRTB	OFF	Boot Block Write Protection bit	Boot block (000000-0007FFh) not write-protected
	1	WRTD	OFF	Data EEPROM Write Protection bit	Data EEPROM not write-protected
CONFIG7L	0F	-	-	-	-
	1	EBTR0	OFF	Table Read Protection bit	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks
	1	EBTR1	OFF	Table Read Protection bit	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks
	1	EBTR2	OFF	Table Read Protection bit	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks
	1	EBTR3	OFF	Table Read Protection bit	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks
ONFIG7H	40	EBTRB	OFF	Boot Block Table Read Protection bit	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

SFRs

SFR values [v1.0]

Address	Name	R/W	Hex	Binary	Description
F80	PORTA	R	xx	1x0x xxx0	Status of Port A… Used for I/F w/ PGA2310 (BD4:U7)
F81	PORTB	R	0x	0000 0xxx	Status of Port B… Used for relays (BD4:RL1-6)
F82	PORTC	R	x0	00x0 0000	Status of Port C… RC5 is controlled by F/W. The other bits are always '0'
F84	PORTE	R	00	0000 0000	Status of Port E pins. Always 00h because Port E is disabled
F89	LATA	R/W	4E	0100 1110	Latch for Port A… Initial state of I/F w/ PGA2310
F8A	LATB	R/W	1x	0001 0xxx	Latch for Port B… Used for relays (BD4:RL1-6), RB4=1 for int
F8B	LATC	R/W	x0	00x0 0000	Latch for Port C… RC5 is used to blink LED
F92	TRISA	W	A1	1010 0001	Tristate control for Port A… RA1-4,6 are outputs
F93	TRISB	W	FB	1111 1000	Tristate control for Port B… RB0-2 are outputs
F94	TRISC	W	DB	1101 1011	Tristate control for Port C… RC2,5 are output
F9B	OSCTUNE	W	00	0000 0000	Default
F9D	PIE1	W	39	0011 1001	Rx/Tx int enable, MCCP (I2C) int enable
F9E	PIR1	R/W	00	00xx 000x	Peripheral interrupt request flag
F9F	IPR1	W	CE	1100 1110	Peripheral interrupt priority… UART, TIMER1 in low priority
FA0	PIE2	W	x0	000x 0000	Interrupt enable… <4>:EEPROM int enable
FA1	PIR2	R/W	x0	000x 0000	Peripheral interrupt request flag… <4>:EEPROM int flag
FA2	IPR2	W	EF	1110 1111	Peripheral interrupt priority…EEPROM in low priority
FA6	EECON1	R/W	0x	0000 xxxx	EEPROM control… Control EEPROM accesses
FA7	EECON2	W	xx	xxxx xxxx	EEPROM control… Write 55h and 0AAh before writing data
FA8	EEDATA	R/W	xx	xxxx xxxx	EEPROM data… Data written to or read from EEPROM
FA9	EEADR	W	xx	xxxx xxxx	EEPROM address… Written before read/write
FAB	RCSTA	W	90	1001 0000	Serial port receive status and control… Serial port enable
FAC	TXSTA	W	26	0010 0110	Serial port transmit status and control… Transmit disable Bit-5 (TXEN) is set after related registers are initialized)
FAD	TXREG	W	xx	xxxx xxxx	EUSART transmit register
FAE	RCREG	R	xx	xxxx xxxx	EUSART receive register
FAF	SPBRG	W	19	0001 1001	Serial port baud rate generator… 19,200bps
FB0	SPBRGH	-	xx	xxxx xxxx	Serial port baud rate generator high byte… Don't access
FB1	T3CON	W	00	0000 0000	Timer control… default
FB2	TMR3L	-	xx	xxxx xxxx	Timer3 register low byte… Don't access
FB3	TMR3H	-	xx	xxxx xxxx	Timer3 register high byte… Don't access
FB4	CMCON	W	07	0000 0111	Comparator control… Default
FB5	CVRCON	W	00	0000 0000	Comparator voltage reference… Default
FB6	ECCP1AS	W	00	0000 0000	ECCP auto-shutdown control… Default
FB7	PWM1CON	W	00	0000 0000	PWM dead-band delay… Default
FB8	BAUDCON	W	02	0000 0010	Baud rate control… Enable receive wake-up
FBA	CCP2CON	-	xx	xxxx xxxx	CCP2 control… Don't access
FBB	CCPR2L	-	xx	xxxx xxxx	Capture/compare/PWM register 2 low byte… Don't access
FBC	CCPR2H	-	xx	xxxx xxxx	Capture/compare/PWM register 2 high byte… Don't access
FBD	CCP1CON	W	0C	0000 1100	CCP1 control… PWM mode, LSBs of duty cycle (Set after T2CON)
FBE	CCPR1L	W	64	0110 0100	Capture/compare/PWM register 1 low byte… MSBs of duty cycle
FBF	CCPR1H	-	xx	xxxx xxxx	Capture/compare/PWM register 1 high byte… Don't access
FC0	ADCON2	W	21	0010 0001	A/D control 2… T_{ACQ}=8*T_{AD}, Clock=F_{OSC}/8
FC1	ADCON1	W	0E	0000 1110	A/D control 1… Port configuration (AN0 only)
FC2	ADCON0	W	0x	0000 00xx	A/D control 0… <1:0> are set in driver
FC3	ADRESL	-	xx	xxxx xxxx	A/D result low byte… Don't access
FC4	ADRESH	-	xx	xxxx xxxx	A/D result high byte… Don't access
FC5	SSPCON2	R/W	xx	0xxx xxxx	MSSP control 2… control Tx/Rx during communication
FC6	SSPCON1	R/W	28	0010 1000	MSSP control 1… Enabled as I^2C Master Mode
FC7	SSPSTAT	R/W	80	1000 0000	MSSP status (I^2C)… Standard speed (100kHz)
FC8	SSPADD	W	13	0001 0011	MSSP clock frequency… 100kHz

FC9	SSPBUF	R/W	xx	xxxx xxxx	MSSP Receive/Transmit buffer
FCA	T2CON	W	04	0000 0100	Timer2 control… Enabled, prescale=1:1 (Set after PR2, CCPR1L)
FCB	PR2	W	C8	1100 1000	Timer2 period… =200, 100[usec], 10[kHz]
FCC	TMR2	-	xx	xxxx xxxx	Timer2… Don't access
FCD	T1CON	R/W	9x	1001 000x	Timer1 control… Used as 16-bit timer, prescale 1:2
FCE	TMR1L	R/W	xx	xxxx xxxx	Timer1 low byte
FCF	TMR1H	R/W	xx	xxxx xxxx	Timer1 high byte
FD0	RCON	W	DF	1101 x111	Reset control… Enable interrupt priority level, WDT flag
FD1	WDTCON	W	00	0000 000x	Watch dog timer control… Enable WDT at the end of initialize
FD2	HLVDCON	W	05	0000 0101	High/low voltage detect control… Default (disable)
FD3	OSCCON	R/W	72	0111 0010	Oscillator control… Internal oscillator, 8MHz
FD5	T0CON	W	C3	1100 0011	Timer0 control… Enable, 8-bit, 1/16 prescale
FD6	TMR0L	W	81	1000 0011	Timer0 low byte… 1msec interval
FD7	TMR0H	-	xx	xxxx xxxx	Timer0 high byte… Don't access
FD8	STATUS	R	xx	xxxx xxxx	Status… Don't access
FD9	FSR2L	-	xx	xxxx xxxx	FSR2 (Data memory pointer) low byte… Don't access
FDA	FSR2H	-	xx	xxxx xxxx	FSR2 (Data memory pointer) high byte… Don't access
FDB	PLUSW2	-	xx	xxxx xxxx	Not physical register
FDC	PREINC2	-	xx	xxxx xxxx	Not physical register
FDD	POSTDEC2	-	xx	xxxx xxxx	Not physical register
FDE	POSTINC2	-	xx	xxxx xxxx	Not physical register
FDF	INDF2	-	xx	xxxx xxxx	Not physical register
FE0	BSR	-	xx	xxxx xxxx	Bank select… Don't access
FE1	FSR1L	-	xx	xxxx xxxx	FSR1 (Data memory pointer) low byte… Don't access
FE2	FSR1H	-	xx	xxxx xxxx	FSR1 (Data memory pointer) high byte… Don't access
FE3	PLUSW1	-	xx	xxxx xxxx	Not physical register
FE4	PREINC1	-	xx	xxxx xxxx	Not physical register
FE5	POSTDEC1	-	xx	xxxx xxxx	Not physical register
FE6	POSTINC1	-	xx	xxxx xxxx	Not physical register
FE7	INDF1	-	xx	xxxx xxxx	Not physical register
FE8	WREG	-	xx	xxxx xxxx	Working register… Don't access
FE9	FSR0L	-	xx	xxxx xxxx	FSR0 (Data memory pointer) low byte… Don't access
FEA	FSR0H	-	xx	xxxx xxxx	FSR0 (Data memory pointer) high byte… Don't access
FEB	PLUSW0	-	xx	xxxx xxxx	Not physical register
FEC	PREINC0	-	xx	xxxx xxxx	Not physical register
FED	POSTDEC0	-	xx	xxxx xxxx	Not physical register
FEE	POSTINC0	-	xx	xxxx xxxx	Not physical register
FEF	INDF0	-	xx	xxxx xxxx	Not physical register
FF0	INTCON3	W	C0	1100 0000	External interrupt control… disable(default)
FF1	INTCON2	W	F5	1111 0101	External and Timer0 interrupt control… Default
FF2	INTCON	R/W	Ex	1110 x00x	Interrupt control… enable interrupts, TMR0 int enabled, RB int enabled
FF3	PRODL	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF4	PRODH	-	xx	xxxx xxxx	Product of multiply low byte… Don't access
FF5	TABLAT	-	xx	xxxx xxxx	Program memory table latch… Don't access
FF6	TBLPTRL	-	xx	xxxx xxxx	Program memory table pointer low byte… Don't access
FF7	TBLPTRH	-	xx	xxxx xxxx	Program memory table pointer high byte… Don't access
FF8	TBLPTRU	-	xx	xxxx xxxx	Program memory table pointer upper byte… Don't access
FF9	PCL	-	xx	xxxx xxxx	Program counter low byte (also defined as PCLAT)… Don't access
FFA	PCLATH	-	xx	xxxx xxxx	Program counter latch low byte… Don't access
FFB	PCLATU	-	xx	xxxx xxxx	Program counter latch upper byte… Don't access
FFC	STKPTR	-	xx	xxxx xxxx	Stack pointer… Don't access
FFD	TOSL	-	xx	xxxx xxxx	Top-of-stack low byte… Don't access
FFE	TOSH	-	xx	xxxx xxxx	Top-of-stack high byte… Don't access
FFF	TOSU	-	xx	xxxx xxxx	Top-of-stack upper byte… Don't access

Internal Specifications

Soft timers

Soft timer is counted down by Timer0 interrupt which occurs every 1msec.
main() sets the initial value to each soft timer, and check the value in the main loop. If the value is zero, it means the time is out.

Three Soft timers are defined:

Soft timer	Definition	Period	Description
CntTickDiag	Tick for test program	1[sec]	Let test program advance to next step
CntTickMain	Tick for main function	100[msec]	Notify timing of reading VR1 and SW2 to tasks
CntTimeout	Timeout for display	3[sec]	Notify timeout to display driver

EEPROM usage

EEPROM holds the following data:

Address	Name	Description
0	OffsetL	Right channel offset – low byte
1	OffsetH	Right channel offset – high byte
2	DispMode	Display mode
3	Inten	Intensity level
4	Check sum	Check sum for sum check

[END OF DOCUMENT]